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EDN

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEER

Multibus I/O-board directory

Software performance analyzers

Comparators

ISSCC preview

stands alone.

error correction technique, the ICL7134 provides up to 14 bits of accuracy and ultra-high stability over the entire operating temperature range. Plus the same cool low-power CMOS performance.

Right now, we've got plenty of stock available. So once you see how easily the ICL7115 interfaces to your hardwired system and hooks up to 8- or 16-bit buses, you can spec the A/D chip that stands without peer.

Matter of fact, give us a call today and we'll put this super A/D converter in your hands. After all, we designed the ICL7115 for great engineers. Like you.

Call us for your free evaluation ICL7115, or write Intersil, Inc., Mail Stop R1-26, 10600 Ridgeview Court, Cupertino, CA 95014. In Europe, call (02) 673-93-79 or 660-20-14. Or write General Electric, International Operations, Chaussee de la Hulpe, 150-Bte. 5, 1170 Brussels, Belgium.

And discover—first hand—why GE stands for Great Engineering.

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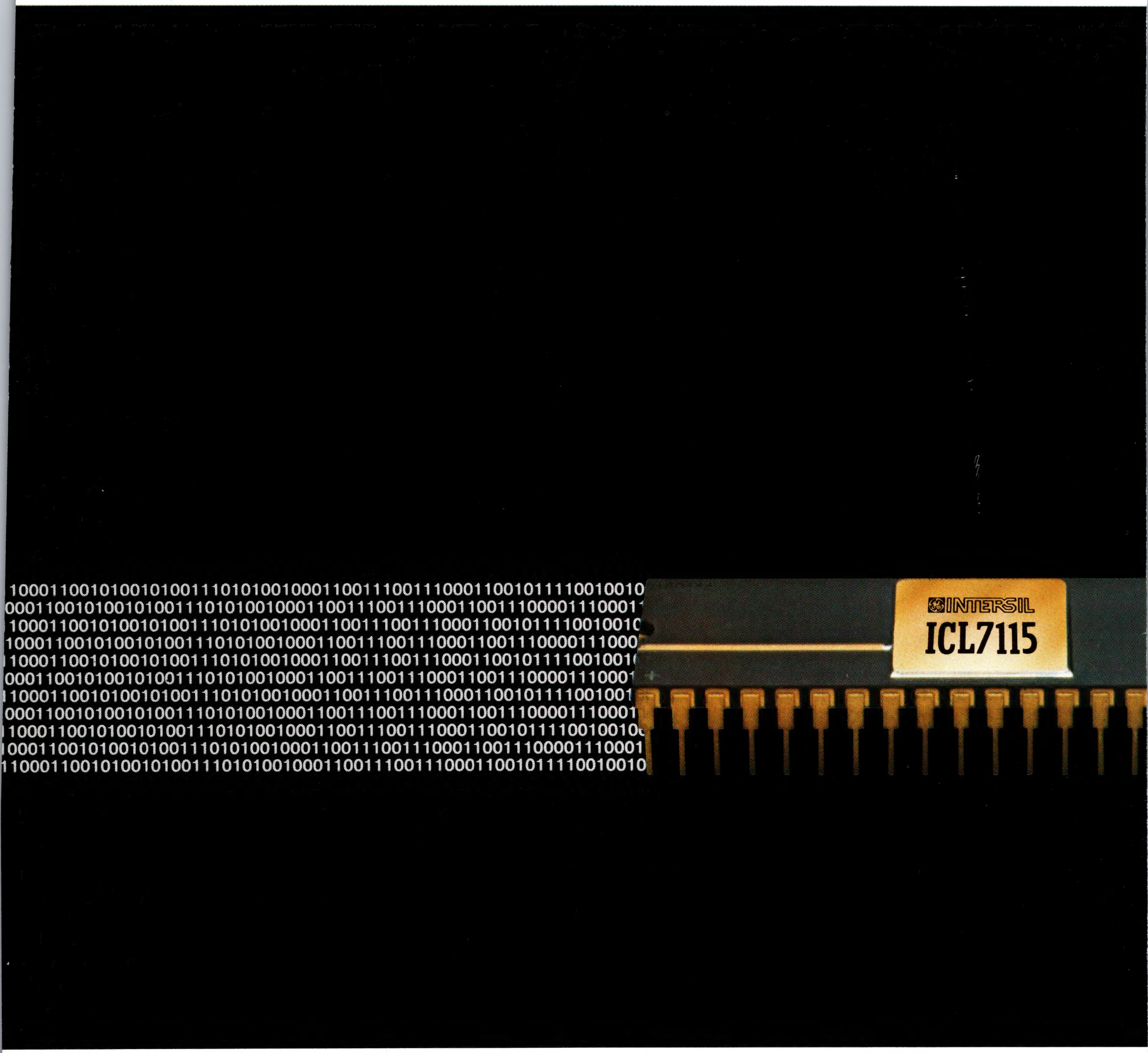
Ext. 428. Free evaluation ICL7115s are available to the first 3000 qualified callers.

Our ICL7115



The only 14-bit monolithic A/D converter on the market today—that's Intersil's ICL7115. It's the chip that will change the definition of signal processing.

Data acquisition and data logging applications are a whole new ball game with the ICL7115. It's monolithic, which means lower cost and higher reliability than systems built with hybrids or modules. And its successive approximation technique gives you 25,000 conversions per second, for more rapid sampling and greater digitizing capabilities.

The key to the ICL7115 is our proprietary EPROM error correction technique. Unlike conventional techniques such as laser trimming, this unique EPROM correction method compensates for linearity and full-scale error with greater precision and stability, over the entire operating temperature range.

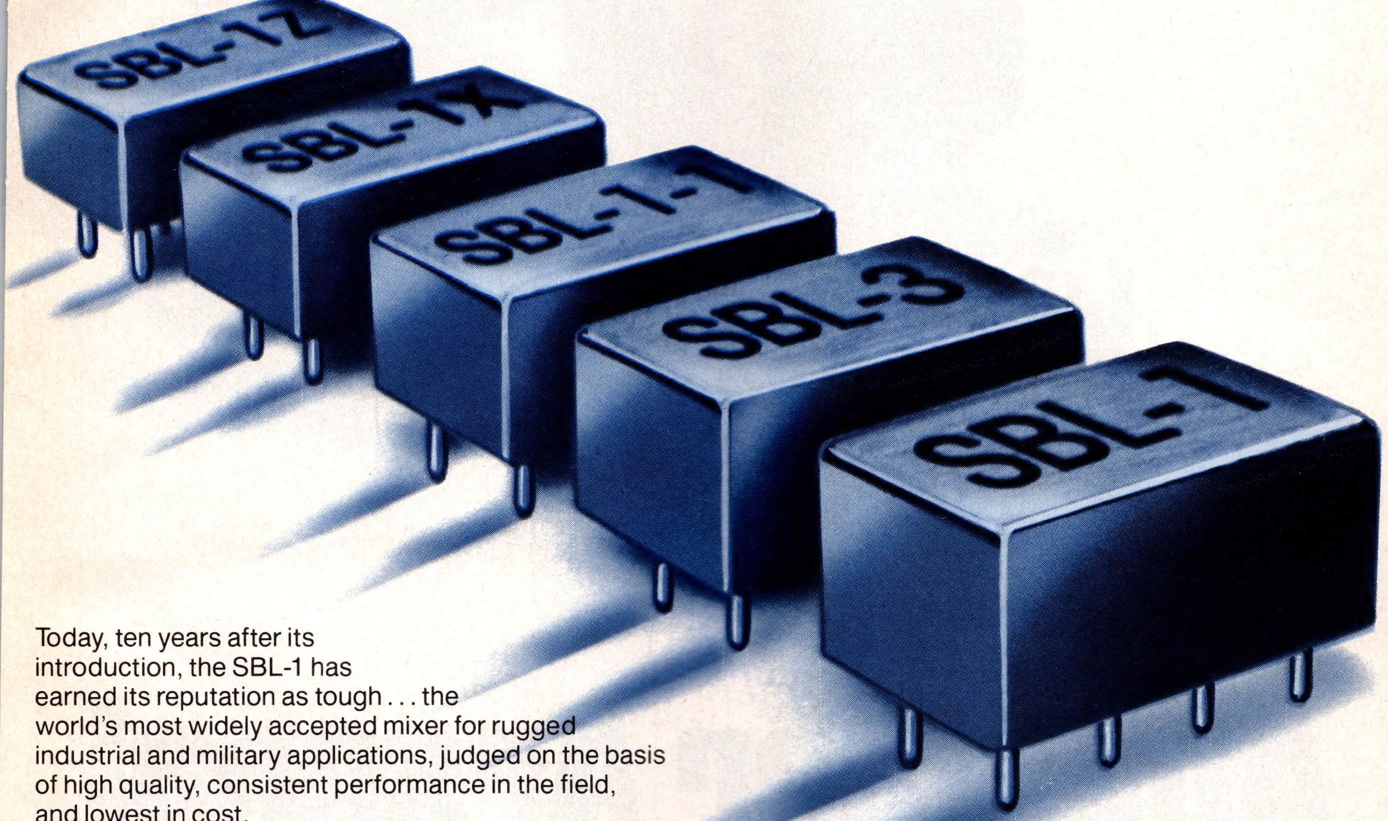
Though it's a hot new product, the ICL7115 is a very cool performer: thanks to our advanced CMOS technology, the whole package dissipates only 10mW.

And if your system requires equal precision in a D/A converter, our ICL7134 meets the challenge. Utilizing the same proprietary EPROM

CIRCLE NO 18

GE stands for Great Engineering in analog signal processing:

more tough mixers



Today, ten years after its introduction, the SBL-1 has earned its reputation as tough . . . the world's most widely accepted mixer for rugged industrial and military applications, judged on the basis of high quality, consistent performance in the field, and lowest in cost.

And the winning formula is not a secret.

Using the latest automated production and test equipment available, Mini-Circuits stress tests each individual component before assembly and then subjects each assembled SBL-1 to 17 grueling tests before acceptance, date coding and close checking for unit-to-unit repeatability.

The SBL-1 does have one drawback however. It only covers 1 to 500 MHz. That's why we've expanded the product family with additional models to cover 25 KHz to 1000 MHz. The new units are assembled with the same production and test expertise as the SBL-1; that's why we can offer 0.1% AQL on all SBL models . . . no rejects, not a single one, on every order shipped. So don't compromise your design or settle for a poor imitation. Specify Mini-Circuits SBL Mixers.

For full specifications call or write for latest RF/IF Signal Processing Handbook or refer to EEM, Gold Book, or Microwaves Directory.

SBL SPECIFICATIONS (typ.)

Model	Freq. (MHz)	Conv. Loss	Isolation,dB L-R	Isolation,dB L-I	Price (10-49)
SBL-1	1-500	5.5	45	40	**$4.50**
* SBL-1X	10-1000	6.0	40	40	**$5.95**
SBL-1Z	10-1000	6.5	35	25	**$6.95**
SBL-1-1	0.1-400	5.5	35	40	**$6.50**
SBL-3	0.25-200	5.5	45	40	**$7.50**

* If not DC coupled.

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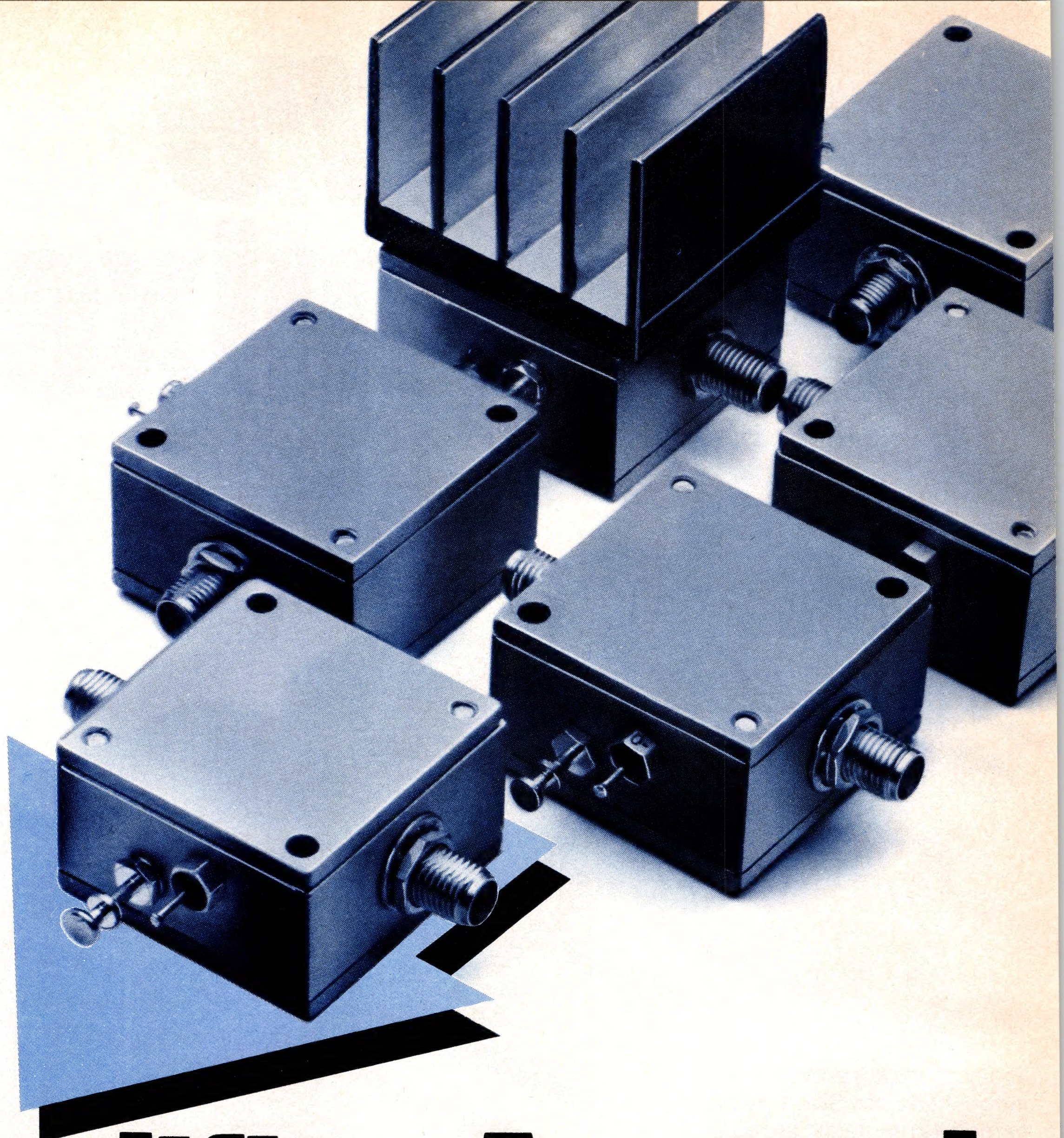

Volume 31, Number 3

EDN

February 6, 1986

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

***On the cover:** Graphics-controller ICs now let you implement raster-graphics systems that achieve fast drawing speeds that previously required the use of bit-slice processors. Moreover, the new controllers make medium- and low-performance graphics systems easier and less expensive to design and build. See pg 104. (Photo courtesy Texas Instruments Corporate Graphics)*

DESIGN FEATURES

Continued on page 7

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If you can't fix your board with the enhanced 9000 Series, it's beyond repair.

Introducing a new dimension of test capabilities for the Fluke 9000 Series Micro-System Troubleshooter line.

Finally there's a way to conquer some of the most difficult board testing problems imaginable. Take control of the situation with Fluke's 9000 Series and new **Asynchronous Signature Probe option.** You'll be able to pinpoint virtually every digital hardware fault on the entire board. Even those frustrating faults in circuits that operate independently of the microprocessor bus cycle.

Begin testing boards with the 9000 Series' built-in, preprogrammed test routines. In a single keystroke, you can automatically check the entire microprocessor kernel—Bus, ROM, RAM and I/O.

For testing beyond the bus, Fluke's new probe option eliminates the need for a logic analyzer or scope to test asynchronous circuits. One complete package, easily installed into either new *or* existing 9000 Series units, offers signature analysis, waveform capture and event counting. These three vital troubleshooting functions give *any* 9000 Series the power to diagnose:

- DMA Controllers
- Disk Controllers
- Video Controllers
- Video-Generation Circuits
- Communication Circuits
- Peripheral Controllers
- Dynamic RAM timing relationships

Not only does the 9000 Series test more of the board, it also supports more 8-bit and 16-bit processors than any other tester on the market.

Call Fluke toll-free **1-800-426-0361** or contact your local representative, and put your most challenging board to the 9000 Series test. If it can't be fixed with the enhanced 9000, it's probably beyond repair.

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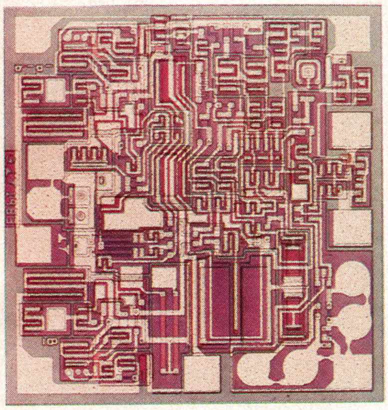
EDN

February 6, 1986



Monolithic comparators offer impressive specs, but the devices' high gain and wide bandwidth can combine to make their behavior temperamental (pg 45).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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Continued from page 7

EDITORIAL

For once, the hardware folks and the software folks are cooperating in a way that'll benefit all of us. The result of this cooperation? The Computer Graphics Interface.

NEW PRODUCTS

PROFESSIONAL ISSUES

Word-processing software, not a CAE package, is an engineer's most valued assistant

LOOKING AHEAD

1990 connector market to top $7.5 billion . . . Market for 32-bit μPs may reach $1B by 1990.

DEPARTMENTS

BPA ABP
Cahners Publishing Company ☐ Publishers of specialized business magazines in Building & Construction ☐ Electronics & Computers ☐ Foodservice ☐ Manufacturing ☐ Medical/Health Care ☐

INMOS introduces the transputer family. A range of evaluation boards for the first transputers is available now.

The transputer is a fast, easy to use VLSI component designed for applications ranging from single microprocessor systems to supercomputers.

The IMS T414 is the first transputer, integrating a 32 bit microprocessor, four inter-transputer communication links, 2 Kbytes of RAM, a 32 bit memory interface and a memory controller onto a CMOS chip.

The microprocessor runs at 10 MIPS and is designed specifically for the execution of high level languages. It combines direct support for multi-tasking, floating point, block transfer and record handling with sub-microsecond procedure call and task switching.

Each transputer link provides a full duplex, 10 Mbits/sec, point to point connection with an on chip DMA controller. Links are used for inter-transputer communication or, via an INMOS Link Adaptor, interfacing to industry standard byte wide peripherals.

The memory interface provides access to a linear 4 Gbyte address space at a data transfer rate of up to 25 Mbytes/sec.

Transputers are designed for ease of engineering. All transputer family devices operate from a single 5 MHz clock input, which is used to derive high speed internal clocks for all on chip systems.

When transputers are directly connected via links, additional components are not necessary. Independent or common clocking can be used, regardless of timing skew.

The configurable memory controller also requires no external components. It provides all the necessary timing and refresh signals for memory systems, comprising any mix of ROM, SRAM, DRAM and memory mapped peripherals.

Transputers are designed for ease of programming. INMOS offers development systems which provide integrated editing, compiling and source level debugging for both single and multiple transputer applications, using C, Pascal, Fortran and occam.

In applications requiring only a single computing element, the transputer's speed, minimal support component requirements and programming efficiency provide significant cost/performance advantages over conventional microprocessors.

Systems of any size can be built from interconnected transputers, using the links. The same program can be configured to run on one, tens or thousands of transputers allowing a simple trade off between performance and cost.

The transputer family already includes 32 bit and 16 bit transputers, peripheral controllers, evaluation boards and development tools. Start assessing its capability for yourself now with an IMS T414 evaluation board.

INMOS Corporation, P.O. Box 16000, Colorado Springs, Colorado 80935, USA. Tel: (303) 630-4000. Tx: (910) 920-4904
INMOS Limited, Whitefriars, Lewins Mead, Bristol, U.K. BS1 2NP. Tel: 0272 290861 Tx: 444723.
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TRANSPUTER PRODUCTS	
IMS T414	**32 Bit, 2 Kbyte RAM, 4 Transputer links**
IMS T212	**16 Bit, 2 Kbyte RAM, 4 Transputer links**
IMS C001	Transputer Link Adaptor, Separate 8-Bit input and output
IMS C002	Transputer Link Adaptor, Multiplexed 8-Bit input/output

DEVELOPMENT TOOLS	
IMS D100	INMOS Transputer Development System
IMS D600	Transputer Development Software, VAX-VMS
IMS D700	Transputer Development Software, IBM-PC

EVALUATION BOARDS	
IMS B001	Double Eurocard, IMS T414, 64 Kbyte RAM, 2 x RS232C ports
IMS B002	Double Eurocard, IMS T414, 2 Mbyte RAM, 2 x RS232C ports
IMS B004	IBM-PC add on card, IMS T414, 1 Mbyte RAM

For a complete data pack on the Transputer and its support products, fill in the response coupon, and post to INMOS Corporation P.O. Box 16000 Colorado Springs, Colorado 80935, USA.
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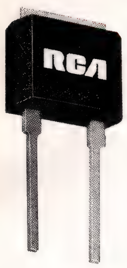


A breakthrough in surge protection.

Now there is something new in the world of surge protection. Surgectors are unlike zeners, MOVs, carbon arrestors or gas discharge devices.

Surgectors respond rapidly and handle a lot of energy. They are ideal for protecting sensitive or expensive components from lightning strikes, load changes, switching transients, commutation spikes, electro-static discharge and line crosses.

How Surgectors work.

Surgectors are monolithic structures integrating a zener diode and an SCR into one reliable, cost-effective device.

At low voltages, the Surgector is "off," representing high forward impedance (only 50nA leakage current). The instant clamping voltage is exceeded, Surgector turns "on." The zener starts to conduct immediately. Current flows from the zener region into the thyristor gate and within nanoseconds the SCR turns on to handle heavy currents. Destructive surges are shunted to ground. Once the voltage surge passes, the Surgector makes a fast transition back to the "off" state.

Five Surgector choices.

Our opening Surgector line-up is three 2-terminal devices (30V, 60V and 230V), one bi-directional (230V) and one 3-terminal (100V).

The 3-terminal Surgector gives you access to the SCR gate lead, allowing the device to be triggered with your voltage level detector.

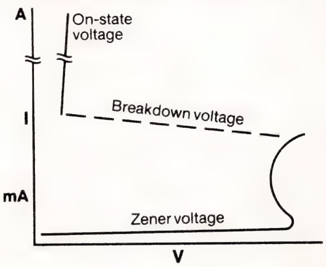
Type		Rating	Price (1K)
SGT03U13	2-terminal	30V	.60
SGT06U13	2-terminal	60V	.62
SGT23U13	2-terminal	230V	.70
SGT23B13	bi-directional	230V	.99
SGT10S10	3-terminal	100V	.72

Surgector vs. zener and MOV.

Surgectors are as fast as zener diodes (<1ns response time) yet can handle ten times as much energy. At breakdown voltage, Surgectors are two orders of magnitude lower in impedance than zeners (0.1 ohm vs. 10 ohms).

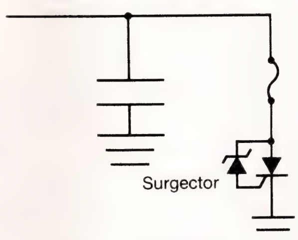
Compared with MOVs, Surgectors have a much better clamping ratio. An MOV with operating voltage of 100V may allow a 300V surge before it offers any protection. A 100V Surgector turns "on" with only a 110V surge. Surgectors are ten times faster, dissipate much less power and have longer lives than MOVs.

Typical Surgector voltage-current characteristics.



Surgectors are much faster than gas discharge tubes or carbon arrestors, but can carry less surge current. The transient peak current capability of the Surgector is 300A for 1μs x 2μs pulse and 75A for a 10μs x 1000μs pulse. Like other surge protectors, Surgectors will eventually fail if pushed beyond specifications. But Surgectors normally fail shorted, rather than open. And even shorted Surgectors protect expensive components. Only beyond triple the rated surge current will the Surgector blow open.

Typical protection for expensive components.



For more information on Surgectors, call our Power Application Hotline (800-RCA-APPL), your RCA sales office or distributor, or write: RCA Solid State, Box 2900, Somerville, NJ 08876.

Call: Hamburg, 49-4106-6130; London, 44-93-2785511; Paris, 33-3-946-5656; Hong Kong, 8-52-3-723-6339; Sao Paulo, 55-11-210-4033.

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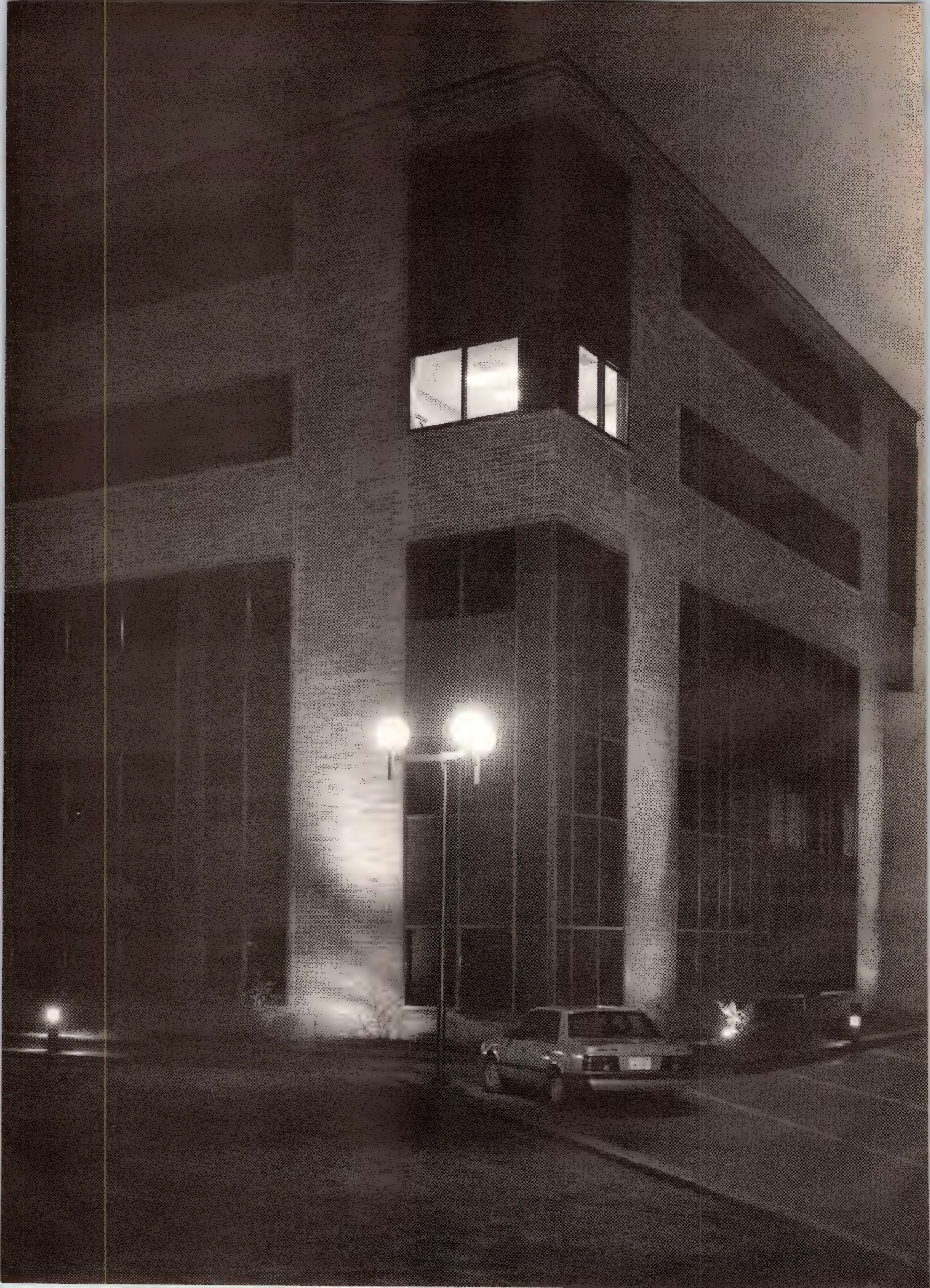


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NEWS BREAKS

EDITED BY JOAN MORROW

PC SOFTWARE HELPS IMPLEMENT μP, PLA, AND GATE-ARRAY DESIGNS

The Master schematic logic analyzer and companion products provide engineers with an economical design tool that allows you to translate schematics into μP-based, PLA-based, or gate-array designs. Aldec-Automated Logic Design Co (Newbury Park, CA, (805) 499-6867) offers Master and a suite of options that includes graphics schematic capture, Alice (Aldec logic in-circuit emulator), the Logic Networking Compiler, and various libraries. System prices range from $3000 for just the Master logic analyzer to $12,000 with all of the software options.

The software executes on the IBM PC, and the graphics option requires the IBM Enhanced Graphics Adapter. Using Master, you can enter schematics, simulate your design, and compile the design into μP object code, PLA program files, or Fujitsu-compatible gate-array files. The Alice hardware/software package allows you to connect the design you created on the PC to its intended hardware environment, enabling you to debug your design before building it. For μP-based systems requiring more than one μP, you can use the Logic Networking Compiler to produce object code for multiple μPs operating in parallel.—Maury Wright

DIGITIZING OSCILLOSCOPE CAPTURES 300-MHz REPETITIVE SIGNALS

With Hewlett-Packard's $17,600 54100A digitizing oscilloscope, you can view repetitive signals to 1 GHz. However, it limits your viewing of single-shot events to 10 MHz because of its 40M-sample/sec digitizing rate. The company's $7900 54200A lets you view 50-MHz single-shot events (200M-sample/sec digitizing rate). It limits your viewing of repetitive events to 50 MHz because it doesn't use a repetitive sampling technique to digitize the waveform. Instead of an either/or choice of a scope with high single-shot bandwidth or a scope with high repetitive frequency, you can choose HP's 54201—a 300-MHz scope with a 200M-sample/sec digitizer.

Specifically, a 300-MHz front end and repetitive-sampling circuitry was added to the 54200. The scope uses a random repetitive-sampling technique to capture and display pretrigger data. Two models are included in the 54201 Series: the 54201A ($7900) and the 54201D ($9800). The D model has all the measurement capabilities of the A plus additional triggering capabilities for triggering the scope with digital circuitry.

In addition to the increase in repetitive signal-measurement bandwidth from 50 to 300 MHz, the 54201 has several other feature enhancements over the 54200. It can save the maximum, minimum, and mean average time-delay measurement values. This capability is added to the automatic pulse-parameter measurement capability already provided with the 54200. The company has also added waveform math capabilities and a connect-the-dots display mode.—Chris Everett

HANDS-ON COURSE LETS YOU DESIGN AND BUILD GaAs ICs

Triquint Semiconductor's (Beaverton, OR, (503) 629-3126) GaAs-IC design course will teach you how to use the company's IC-design tools to design your own device. You'll also receive prototypes of your design. Running from March 10 to March 13, the course contains two sections: instruction in the use of the company's IC-design tools, and layout and fabrication of your own GaAs chip. The course also covers testing, packaging, and the reliability of GaAs ICs. For $9900, you receive lodging, layout and fabrication services, packaged samples of your design, an evaluation board, class notes, and lunches. To attend, you must respond by March 3, 1986, to Ajit Rode at Triquint Semiconductor.—David Smith

512k-BIT CHIP PACES EXPANDED EPROM FAMILY

Three new EPROMs, including a 512k-bit device, expand the family of nonvolatile memory products from VLSI Technology (San Jose, CA). The 64k-bit VT27C64, the 128k-bit VT27C128, and the 512k-bit VT27C512 join the already available 256k-bit VT27C256 to form, according to the vendor, the industry's first full family of CMOS EPROM products. The company also claims the VT27C512 is the first 512k-bit EPROM built in high-speed, low-power CMOS technology.

Several features suit these EPROMs for low-power, μP-based applications. A chip-enable input allows you to implement a power-down mode. To eliminate bus contention, an output-enable input disables the chip's outputs. Also, the chips spec cycle times of 150 and 250 nsec, making them compatible with most μPs. The 64k-, 128k-, and 512k-bit versions cost $4.50, $7.81, and $15.28 (5000).—David Smith

CMOS FLASH A/D CONVERTERS OPERATE WITH ONE 3 TO 8V SUPPLY

Three CMOS flash A/D converters from Hybrid Systems (Billerica, MA, (617) 667-8700) require only one 3 to 8V supply for operation. The monolithic devices come in commercial or MIL-STD-883 versions and feature sampling rates from 5 to 30 MHz and power consumption no higher than 300 mW. The 6-bit HS9582 parallel flash converter is spec'd for 15-, 25-, or 30-MHz sampling rates; corresponding power consumption ranges from 50 to 200 mW. Linearity error is ±¼ LSB at 15 MHz with a 5 or 8V supply. An overflow bit allows higher resolution by connecting two converters in series. The HS9582 costs $15.40 to $89 (100).

The 8-bit HS9583 is a 2-step flash device that converts the first three MSBs, and then converts the remaining five LSBs in a second pass. Offering 5- or 10-MHz sampling rates and 75-mW power consumption, it features ±¼-LSB linearity at 5 MHz with a 5 or 8V power supply. Housed in a 24-pin DIP, the devices costs $44.30 to $161 (100). The full-flash 8-bit HS9584 comes in a 28-pin DIP and contains 255 clocked comparators. Offering 10- and 20-MHz sampling rates, this converter specs a 60-psec aperture uncertainty, which allows conversion of full-amplitude signals with frequencies as high as the Nyquist limit. It costs $46.60 to $275 (100).—Tarlton Fleming

68020/80286 DEVELOPMENT TOOLS INCLUDE COPROCESSOR EMULATION

The Tektronix (Beaverton, OR) MultiV Systems package provides design teams with software development tools and hardware/software integration tools for Motorola 68020 and Intel 80286 microprocessors. For software development, Tektronix provides a C language development system (Clands II) and a software execution system (the Software Executer). The hardware/software integration support includes a 68020 emulator and an 80286 emulator. The Clands II package, includes a C compiler, a C language directed editor, a 32-bit macroassembler, a relocating linker, an integration control system, and a C language debugging tool. After you have developed your code on Clands II, you download the code to the MultiV Systems mainframe. You then debug your code on the Software Executer, which contains a 68020 processor and 68881 coprocessor (or 80286 processor and 80287 coprocessor).

The MultiV Systems mainframe can support two Software Executers or two emulators at one time. You can couple them together for multi-emulation support or leave them uncoupled to provide two separate development environments for two users. The 68020 emulator provides real-time transparent emulation of the 16.6-MHz 68020 processor and 68881 coprocessor. The 80286 supports the 10-MHz 80286 processor and 80286 coprocessor. MultiV packages start at less than $20,000.—Chris Everett

If your system is only using this many colors,
isn't it time to grow up?

The INMOS IMSG170 Color Look-up Table offers a grown-up solution to video display color enhancements. It lets you and your RGB analog display advance to a palette of more than a quarter million colors.

This programmable DAC conforms to RS170A standards with pixel rates up to 50 MHz, in a 28 pin package.

And to simplify things, the table integrates the functions of a 256 word x 18 bit color mapping table, three 6-bit DACs, 75 ohm drivers and microprocessor interface into a monolithic CMOS device. The result? Reduced board space and power consumption at a lower cost.

The Color Look-up Table from INMOS. Designing with thousands of colors just became child's play.

INMOS Corporation, Colorado Springs, Colorado, Tel. (303) 630-4000
Bristol, England, Tel. 0272-290-861
Paris, France, Tel. (1) 687-2201
Munich, Germany, Tel. (089) 319-1028

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CIRCLE NO 45

NEWS BREAKS: INTERNATIONAL

EDITED BY JOAN MORROW

JAPANESE IBM-COMPATIBLE COMPUTERS WILL BE SOLD IN US

Toshiba Corp plans to sell its 16-bit T-1100 computer in the United States starting early this year. The company, which sells approximately 5000 of the IBM-compatible portable systems per month in Europe, will initially import 1000 systems per month to the US and sell them through Toshiba America.

CMOS 256k-BIT EPROM FEATURES 120-nSEC ACCESS TIME

The 27C256AD, a CMOS 256k-bit EPROM from Nippon Electric Co, furnishes a 120-nsec access time. The device was designed under a 1.2-μm rule and measures 4.73× 4.45 mm. It consumes 30 mA during operation, 100 μA in standby, and costs ¥1500 ($7.32) (5000).

MOUNTING TECHNIQUE PUTS PACKAGELESS CHIPS ONTO PC BOARD

The Chip On Board (COB) method developed by Ricoh Co allows the insertion of packageless ICs directly onto pc boards. The technology could increase pc-board density two to four times and also reduce production costs by 30%. The company might start using the technology in commercial production next summer.

The COB method employs a sealing resin that has the same protective qualities as conventional plastic or ceramic IC packages. It can be used for memory products, microprocessors, peripheral LSI devices, and gate arrays, and it can reduce the size of equipment such as printers. Many semiconductor vendors were reluctant to supply Ricoh with naked chips, but at least two companies have agreed to help Ricoh with its experimental technique.

SILVER-, GOLD-CONTACT SWITCHES MEASURE 5×2.5×7.5 mm

Suiting such applications as floppy-disk drives, lap computers, car stereos, and portable video cameras, microswitches from Matsushita Electric Works measure 5×2.5×7.5 mm and weigh 0.2g. Approximately one-fifth the size of conventional devices, the microswitches have silver or gold contacts and come in three categories: pin pushbutton, hinge lever, and hinge R lever. They cost ¥120 ($0.59) to $0.66 for silver-contact types and $0.73 to $0.90 for gold-contact versions.

80C88-BASED HANDHELD COMPUTER COSTS $800

The $800 Personal Partner from Panasonic Industrial Co incorporates a 5-line×80-character LCD and is powered by rechargeable NiCd batteries. Built around an 80C88 CMOS μP, the computer provides 8k bytes of RAM, which is expandable to 256k bytes. It also features a resident word-processing program, four read-only memory sockets, and an IBM-style keyboard. An optional bus can accommodate an external printer and a built-in 1200-baud modem.

Nicolet's 800D Logic Analyzer

Because Some Tools Are Indispensable!

No matter where problems are lurking in your digital system, the development and debug measurement capabilities of Nicolet's NPC800D Logic Analysis System help you quickly isolate and dispatch them.

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CIRCLE NO 27

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20dB Stop Band start from	70	135	210	290	410	580	750	800	1000	1100	1340

HIGH PASS **Model PHP**	-50	-100	-150	-200	-300	-400	-500	-600	-700	-800	-900	-1000
Passband, MHz start	41	90	133	185	290	395	500	600	700	780	910	1000
Passband, MHz stop	200	400	600	800	1200	1600	1600	1600	1800	2000	2100	2200
20dB Stop Band, (MHz) from DC to	26	55	95	116	190	290	365	460	520	570	660	720

CIRCLE NO 28

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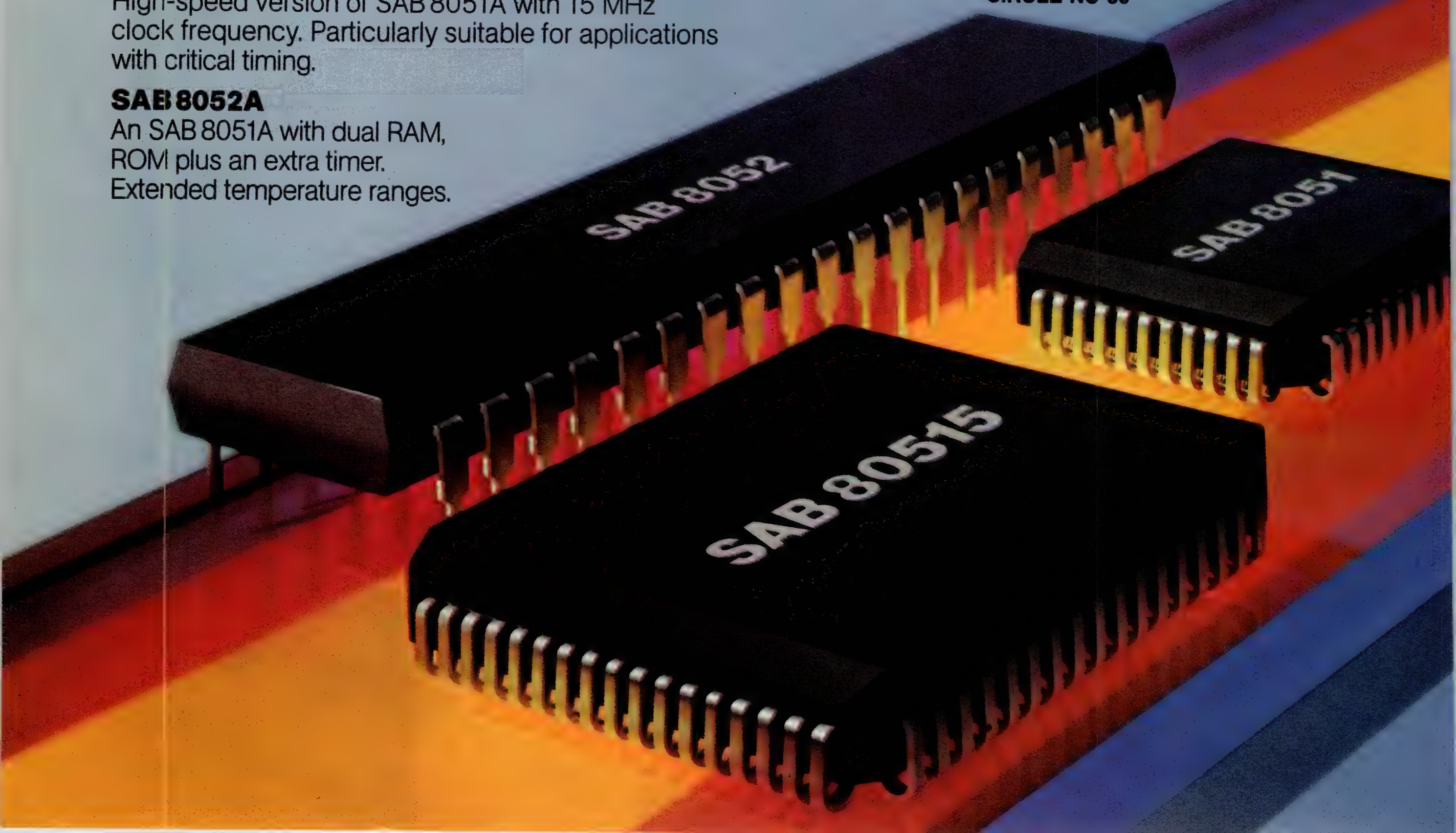
CIRCLE NO 30



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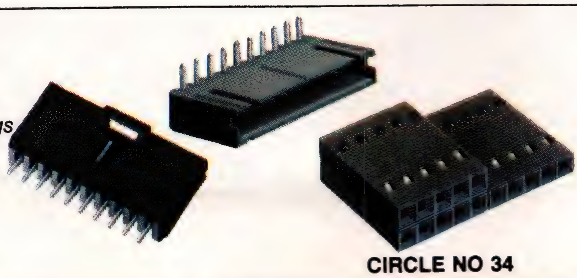

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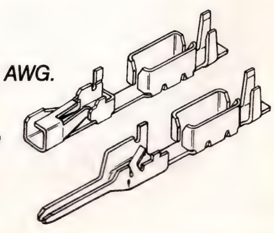
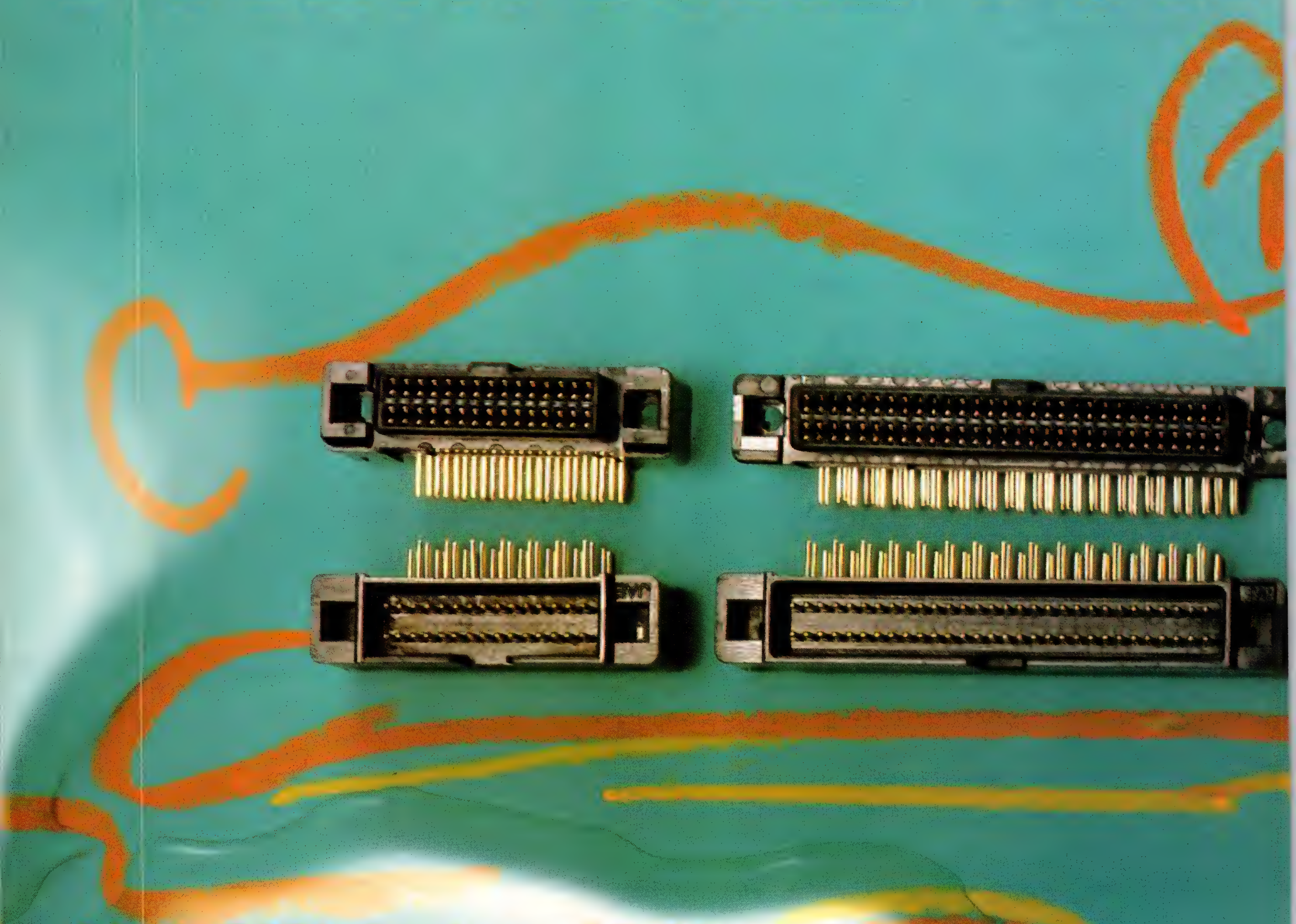


CIRCLE NO 34

PICL...CURE FOR



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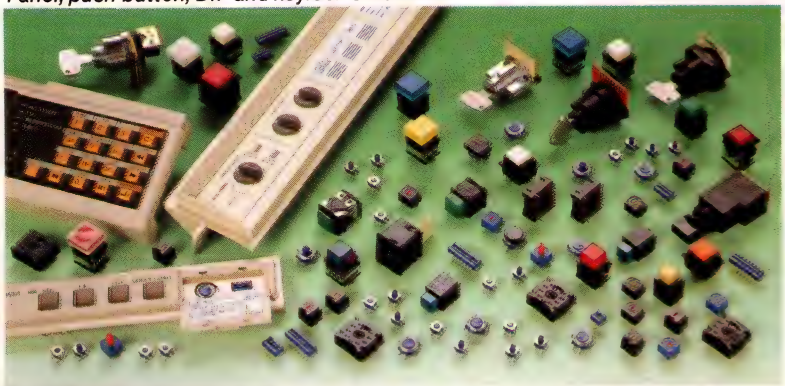

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CIRCLE NO 31

SIGNALS & NOISE

Phantom-component companies commit fraud

Dear Editor:

Oh boy. "The Phantom Component: A science fiction story" (EDN, November 14, 1985, pg 67) has nothing to do with components. The subject is honesty, cheating, and fraud. Appropriate questions to ask readers would be:

I buy components from a cheating, lying, misrepresenting company.

Circle No 521

I am a sucker for a tantalizing sales pitch.

Circle No 522

I look for honesty in the companies I deal with.

Circle No 523

Sincerely yours,
Gus Ositis
Ositis Electronics
Orinda, CA

Engineers need early product information

Dear Editor:

I read your November 14, 1985, editorial on phantom components (EDN, pg 67) with great interest. Phantom components are a real problem. However, limiting information on a new product until a certain number of days before it's available is not the solution. Because of the rapid rate of technological advancement, engineers need as much information as they can get, as early as they can get it, on new products.

Engineers do need to know the new products' status, however. Your editorial staff can play a major role in both determining the significant items that should get readers' attention and providing candid and realistic assessments of companies' claims regarding product availability.

Sincerely yours,
Fan-Chia Tao
Senior Engineer
Kurzweil Computer Products
Cambridge, MA

HP 3852S features 1-μV sensitivity

Dear Editor:

Thank you for reporting on our new HP 3852S data-acquisition system in EDN's October 31, 1985, issue (pg 306). We're glad you found the product's features of interest to your readers.

A small typo did appear in the writeup, however. We at HP's Loveland Instrument Div are the keepers of the microvolt, and when you stated twice that our 5½-digit digital multimeter has 1-mV sensitivity instead of 1-μV sensitivity, you certainly raised the sensitivity level around here.

Sincerely yours,
William S Porter
MARCOM Manager
Loveland Instrument Div
Hewlett-Packard Co
Loveland, CO

Corrections

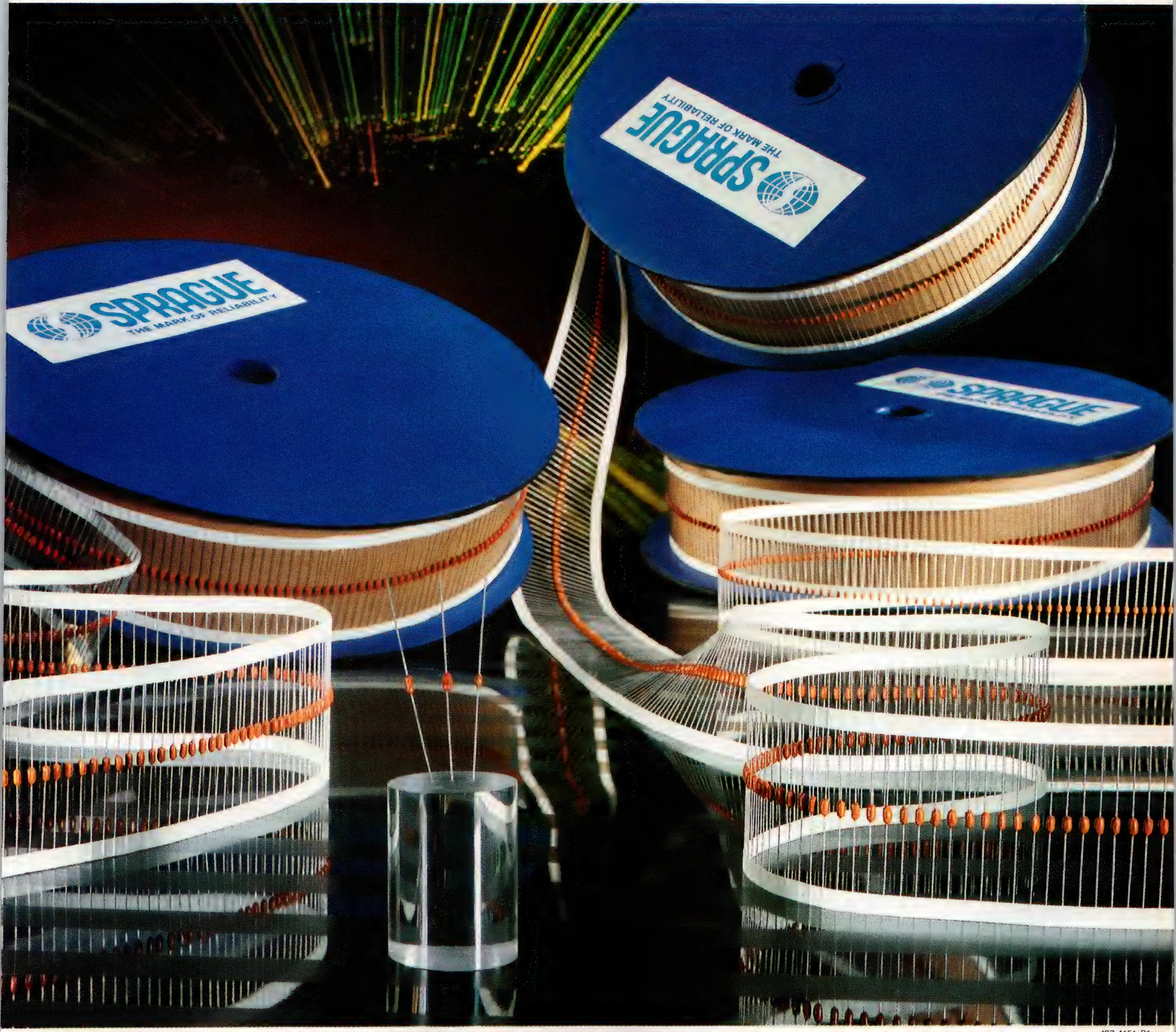
In EDN's 1985 μP/μC Chip Directory (EDN, November 28, 1985, pg 106), the entry for Fairchild's Clipper included the address and phone number for the manufacturer's Microcontroller Div instead of the Advanced Processor Div, which is responsible for the Clipper. For information on the Clipper, please contact:

Fairchild Advanced Processor Div
Fairchild Semiconductor Corp
4001 Miranda Ave
Palo Alto, CA 94304
Phone (415) 858-4361.

One other item of note regarding the Clipper: EDN stated that the cost "should be at least $100 per basic 3-chip set." The official price is $2451.80.

The phone number listed for Metacomp Inc in the November 28, 1985, Product Update on the company's MPA-1000 Multibus Computer (EDN, pg 98) is incorrect. The correct number is (619) 578-9840.

MUCHNESS & QUICKNESS.



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CIRCLE NO 23

CALENDAR

iRMX 86 for Users (short course), Madison, WI. Donna Miller, Micro-Managers Inc, 1435 E Main St, Madison, WI 53703. (608) 251-6661. February 10 to 14.

Grounding and Shielding (short course), San Antonio, TX. Penny Caran, Interference Control Technologies, State Rte 625, Box D, Gainesville, VA 22065. (703) 347-0030. February 18 to 21.

IEEE Annual Meeting, San Jose, CA. IEEE, 10th Fl, 345 E 47th St, New York, NY 10017. (212) 705-7647. February 18 to 19.

IEEE ISSCC '86 (International Solid-State Circuits Conference), Anaheim, CA. Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. (305) 446-8193. February 19 to 21.

AutoCADCon 86, Rosemont, IL. CAD Design Systems Inc, 1305 Remington Rd, Suite D, Schaumburg, IL 60195. (312) 882-0114. February 20 to 21.

C Programming Workshop, Bellevue, WA. Specialized Systems Consultants Inc, Box 55549, Seattle, WA 98155. (206) 367-8649. February 24 to 28.

Nepcon West '86, Anaheim, CA. Banner and Greif, 110 E 42nd St, New York, NY 10017. (212) 687-7730. February 25 to 27.

Compcon Spring, San Francisco, CA. IEEE Computer Society, 1730 Massachusetts Ave NW, Washington, DC 20036. (203) 371-0101. March 3 to 6.

First International Conference on CD ROM, Seattle, WA. Microsoft Corp, Box 97200, Bellevue, WA 98009. (206) 828-8080. March 3 to 6.

Dexpo Europe 86 (DEC-Compatible Exhibition and Conference), London, UK. Expoconsul International Inc, 3 Independence Way,

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Model AD7528
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CIRCLE NO 79

CALENDAR

Princeton, NJ 08540. (609) 987-9400. March 4 to 6.

Power UK '86, London, UK. TCM Expositions Ltd, Exchange House, 33 Station Rd, Liphook, Hampshire, GU30 7DN, UK. (0428) 724660. March 4 to 6.

Design/Drafting with Surface Mount Devices (short course), Milwaukee, WI. Peter Tocups, University of Wisconsin-Milwaukee, 929 N 6th St, Milwaukee, WI 53203. (414) 224-3952. March 5 to 7.

7th Annual Computer Graphics Conference, Hollywood, FL. Frost & Sullivan, 106 Fulton St, New York, NY 10038. (212) 233-1080. March 5 to 7.

CAD/CAM/CAE Winter Workshops, San Diego, CA. Jack Sanders, CAD Report, 841 Turquoise St, Suite D, San Francisco, CA 92109. (619) 488-0533. March 6 to 7.

CIMTECH '86, Boston, MA. Society of Manufacturing Engineers, Box 930, Dearborn, MI 48121. (313) 271-1500. March 10 to 13.

Integrated Services Digital Networks Exposition, Dallas, TX. Information Gatekeepers Inc, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. March 10 to 14.

Structured 8086/186 Assembler (short course), Madison, WI. Donna Miller, Micro-Managers Inc, 1435 E Main St, Madison, WI 53703. (608) 251-6661. March 10 to 14.

Automated Design and Engineering for Electronics (ADEE) West, Moscone Convention Center, San Francisco, CA. Banner and Greif Ltd, 110 E 42nd St, New York, NY 10017. (212) 687-7730. March 11 to 13.

Southcon, Orlando, FL. Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045. (213) 772-2965. March 11 to 13.


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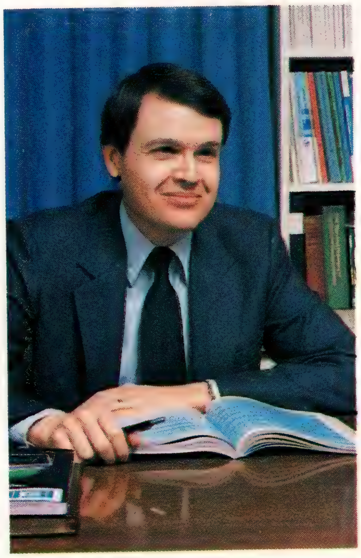
CIRCLE NO 39

Cooperation—at last



Will wonders never cease! The hardware folks and the software folks are actually talking to each other! And they're not even calling each other names! For once, they're cooperating in a way that will benefit all of us.

Their cooperation has resulted in the Computer Graphics Interface (CGI), an interface between hardware and software in graphics systems. CGI is great for software designers, because it defines a rich set of standard, high-level, hardware-independent graphics instructions. It's great for hardware designers, too, because semiconductor manufacturers such as Texas Instruments and Motorola are now implementing it in silicon in their latest graphics-processor ICs. Some of the new chips' instruction sets are actually CGI instructions in off-chip ROM, and they speed up graphics processing enormously. As Southwestern Editor Steve Leibson reports in our cover story (pg 104), graphics systems implemented with the new chips can perform at speeds previously reached only with bit-slice processors.

Semiconductor companies, recognizing that their expertise lies in *implementing* designs in silicon, have been turning to outside experts for help in *specifying* those designs. For CGI, semiconductor giants TI and Motorola turned to the relatively small Graphics Software Systems (Beaverton, OR) and Nova Graphics International (Austin, TX), which specialize in CGI and other graphics software. These software companies helped the IC manufacturers define products that deliver high performance and yet avoid unnecessary difficulty in software development. By providing, in silicon, features desired by software developers, these products obviate the need for special software that converts high-level instructions into low-level command strings.

The high degree of cooperation between hardware and software specialists in developing CGI is commendable, but the benefits of such cooperation needn't be limited to graphics ICs. All digital designs can benefit from such cooperation, and it's high time that regular consultation between hardware and software designers be a part of all projects. Otherwise, we're apt to develop products that do wonderfully what they're *designed* to do, but don't do what anyone *wants* them to do.

Gary Legg

Gary Legg
Editor

THE 68454: THE FIRST TRULY INTELLIGENT DISK CONTROLLER.

What places the new 68454 from Signetics above other disk controllers?

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The 68454 represents some new ideas in disk control technology. Built-in data base management hardware, for instance. It gives you complete control of up to four disks—in any mix of rigid and floppy; *and* it stores disk parameters in a way that speeds and simplifies switching between disk types. Of course, it also comes with all the other features you'd expect in a well-engineered disk controller. On-chip DMA controller and FIFO. Retry/error correction management. It even lets you connect an accessory PLL chip, the 68459, specially designed to link up with the 68454. To give data integrity an extra boost.

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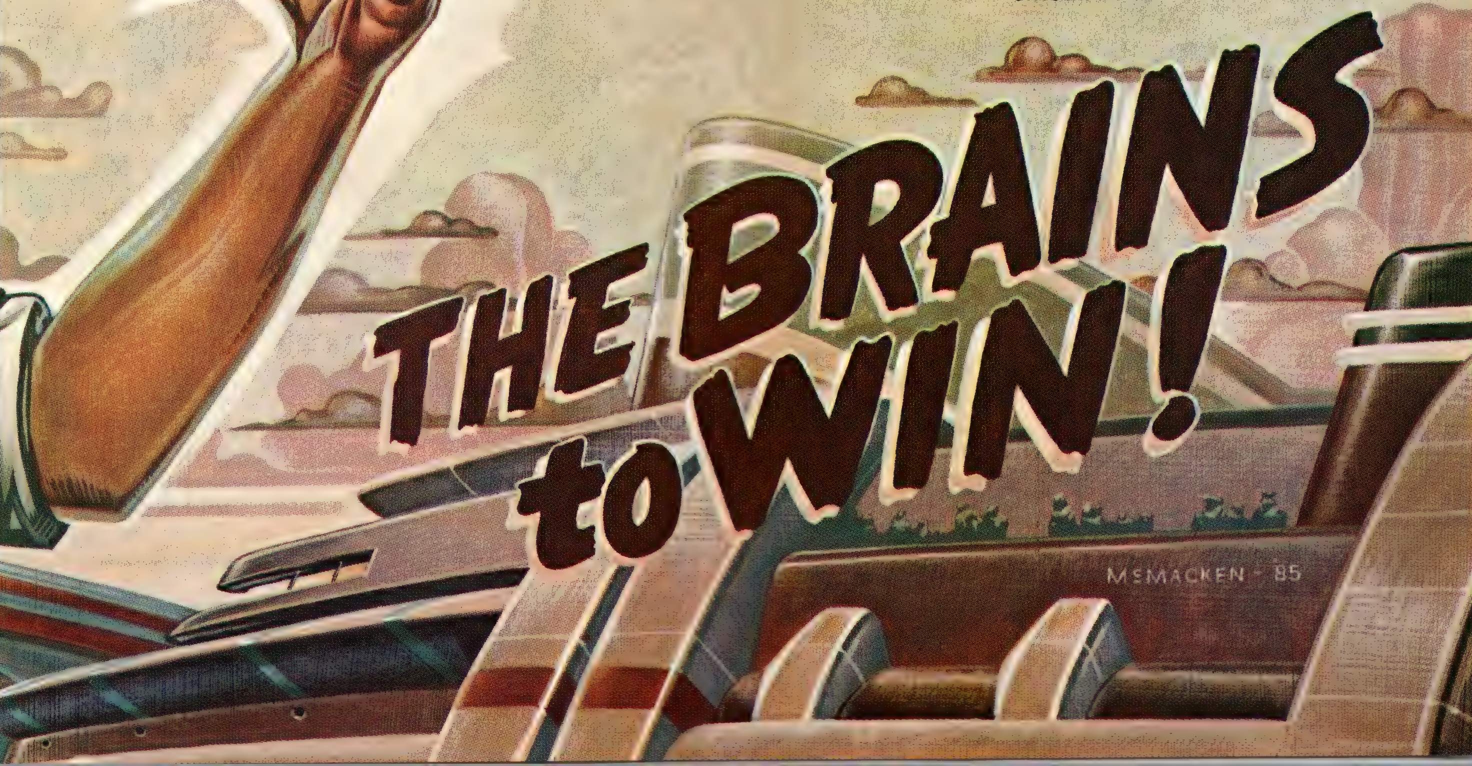
CIRCLE NO 40



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3801401

Design challenges attend application of monolithic voltage-comparator ICs

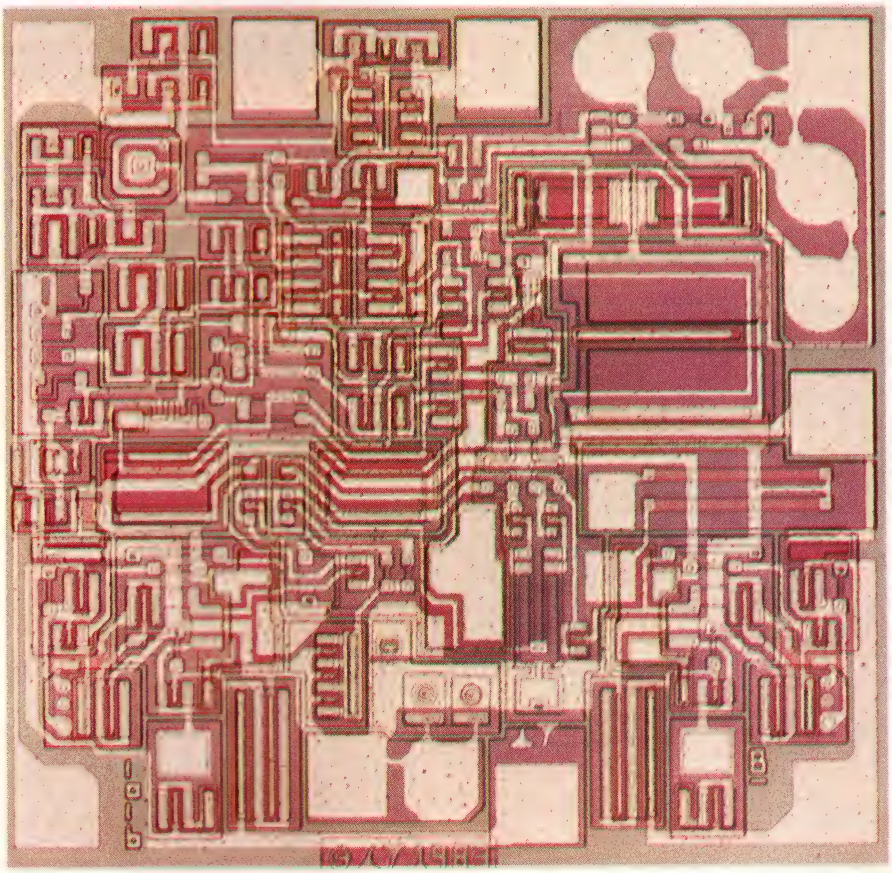
Tarlton Fleming,
Associate Editor

Most of today's comparators are mature, versatile products. You can buy them in a wide range of speeds, but unwelcome characteristics (low gain, high bias current, etc) are prevalent among the older models. The performance of newer devices is impressive, but their behavior remains temperamental, and designing with voltage comparators is still a difficult task. The comparator function demands high gain and wide bandwidth—properties not easily combined on one IC—and the manufacturer's option to trade one for the other is restricted, because the typical application requires both.

One consequence of this inherent design problem is the limited variety of comparator types available (compared, for example, with the wide variety of op amps). Therefore, the best comparator you can choose for a given application is likely to be a rough fit, forcing you to design around the comparator's limitations. Depending on the part, these limitations can include high input bias currents, low gain, narrow common-mode range, nonstandard supply-voltage requirements, and a tendency to oscillate.

You surmount most of these comparator shortcomings at the cost of increased circuit complexity, and your specific added design tasks depend on the type of comparator you initially choose. Comparators fall into three rough categories determined by speed (assuming you set aside a few maverick devices for separate discussion).

At the top end are devices that are based on bipolar ECL and feature propagation delays as short as 2 nsec. With one exception, these comparators come with standard pinouts. Next are the middle-performance comparators, few in number, that attempt to provide as much speed and accuracy as possible in one device. The majority of these are used in A/D converters with 10-bit resolution or better.



Furnishing a 10-nsec propagation delay, *the LT1016 bipolar precision comparator from Linear Technology Corp has latched complementary outputs and offers stability in its linear region of operation.*

In the third category you find most of the comparator population —1-bit A/D converters with response times from 200 nsec to several microseconds. These devices include low supply-voltage versions, low-power versions, FET-input versions, and dual and quad versions. They suit a wider spectrum of applications than many designers realize. Because comparators have a reputation for unpredictable behavior (they might burst into oscillation, blurring their own switching threshold, or they might create spurious pulses by chattering over a decision they have made), engineers are wary of these components and often choose a circuit approach that avoids comparators altogether. The use of comparators can, however, reduce your cost and component count **(Ref 1).**

The fastest voltage comparators

you can buy today are the bipolar-ECL types offered by Advanced Micro Devices, Plessey, Honeywell, Analog Devices, and LeCroy. (All are monolithic; comparators based on hybrid construction methods are generally proprietary designs not offered commercially.) Except for LeCroy's Model MVL407 monolithic quad comparator, the models in this group are all plug-compatible with either the single Am685 or dual Am687 types originally introduced by Advanced Micro Devices.

AMD's Am685, for example, specs a 6.5-nsec max propagation delay at 25°C under the standard test conditions: a 100-mV step with 5-mV overdrive. (Overdrive is the input differential voltage in excess of the value required to drive the output voltage to its logic-threshold value.) The voltage gain—approximately 1600—is fine for use in automatic test equipment (ATE) but generally impractical for use in mass-produced A/D converters. The Am685's 6V, −5.2V supply-voltage requirements are a headache for systems designers, but these nonstandard values are necessary to support ECL-compatible output logic levels (approximately −1.75V and −0.85V).

Supply voltages are less of a problem for the single, TTL-compatible Am686 (5V, −6V) and the dual, ECL-compatible Am687 (5V, −5.2V). Fabricated using a Schottky-clamped bipolar process, all three AMD comparators come in 16-pin DIPs; other package options include an 8-pin DIP, a 20-contact LCC, and a 10-lead metal can. These devices furnish complementary logic outputs and a latch-enable input. The Am687 offers a complementary latch enable as well.

Racehorse comparators

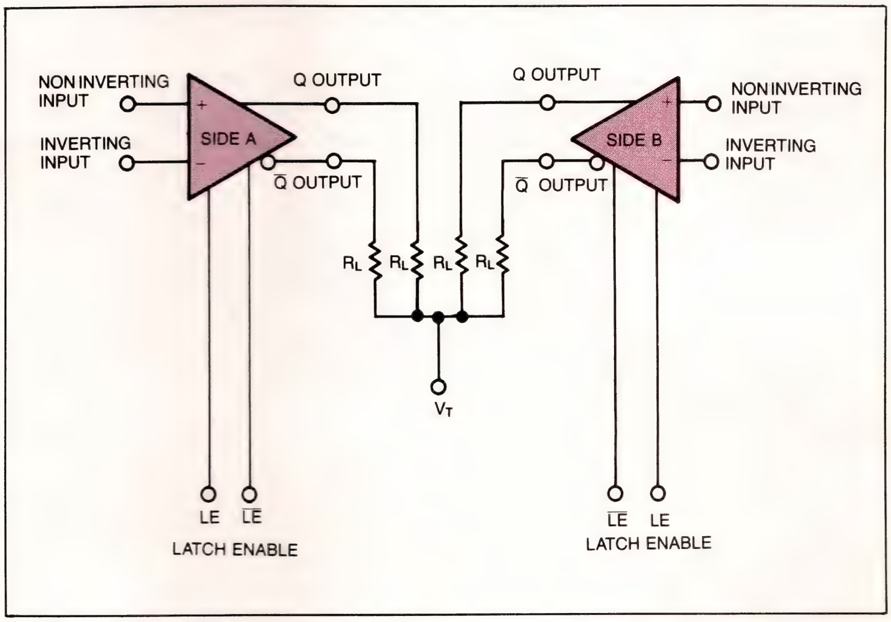
Plessey Semiconductors' SP9685 and SP9687 ECL-compatible comparators spec faster (2.5-nsec) propagation delays. These models and the similar AD9685 and AD9687 from Analog Devices are pin-compatible with the Am685 and Am687, respectively. AMD has answered with the Am6685 and Am6687, comparable to the parts from Plessey, and Honeywell Signal Processing Technologies has recently introduced the HCMP96850 and HCMP96870. All of these second-generation ECL-compatible comparators employ a combination of process and circuit enhancements to achieve response times between 2 and 3 nsec. AMD's proprietary IMOX process, for example, provides shallow-junction ion-implanted transistors with a low junction capacitance and short transit times.

The Honeywell parts' guaranteed differential propagation delay, or skew (±300 psec, input to output; ±200 psec, latch to output), can reduce your system-recalibration requirements, according to product-marketing manager Randel Castelberry. This guarantee applies both to comparators within a package and to comparators in different packages.

All of these very fast comparators require 5V/−5.2V supplies, except the Am6685 (6V/±5.2V). Model MVL407 from LeCroy Research Systems offers similar speed and ECL-compatible outputs but operates from ±5V supplies. The monolithic MVL407 provides four comparators in a 20-pin DIP. Each comparator has complementary outputs, and an internal 3.5-mV hysteresis stage allows comparison of low-level or slowly changing signals without oscillation. Latches are not included in this model.

Speed is key for ATE

The major application for high-speed dual comparators is in ATE systems. Testers of high-pin-count digital ICs in particular use four to eight comparators per pin just to verify digital switching thresholds and to generate timing intervals. Each of these jobs requires two comparators, so the dual units offer convenience, plus the advantage of closely matched electrical parameters that track each other with variations in temperature and supply voltage. You can produce a precise pulse width (time interval), for example, by connecting a NAND gate's inputs to the outputs of two comparators that are fed by the same fast voltage ramp. The pulse width obtained in this way remains unaffected, because each comparator's performance will change by the



***Used primarily in ATE systems,** the Am6687 high-speed comparator has dual complementary latched outputs that are ECL compatible. Propagation delay is less than 3 nsec.*

same amount and in the same direction.

Comparator speed is the main consideration in these ATE applications because it directly affects the tester's throughput rate. Although this speed is obtained at the expense of higher input bias currents, fast comparators can be used as they are in about half of all ATE applications. In the other applications, you must add a FET-input stage or use other means to buffer the comparator's bias current, according to Pete Sylvan, a design engineer for Teradyne Inc. In general, ATE systems can tolerate the moderate gain and high power dissipation associated with fast comparators.

Stable in the linear region

Also in the fast-comparator class is Linear Technology's 10-nsec model LT1016C, which has complementary TTL-compatible latched outputs. The negative supply current is only 3 mA, yielding about 140 mW for total power dissipation —approximately half that of comparable ECL types. In addition, the low input-offset voltage (3 mV max) suits this device to use in successive-approximation A/D converters. What's more, the LT1016C is stable in its linear region—a feature not available in any other high-speed comparator, according to the company. This stability reduces the problem of oscillation when handling slow-moving input signals. Also, of course, it eliminates the

REPRESENTATIVE VOLTAGE COMPARATORS

MANUFACTURER AND MODEL[1]	RESPONSE TIME[2] (nSEC TYP)	VOLTAGE GAIN (V/mV MIN)[3]	INPUT BIAS CURRENT (μA MAX)[3]	INPUT OFFSET VOLTAGE (mV MAX)[3]	DIFFERENTIAL INPUT VOLTAGE (V MAX)	SUPPLY VOLTAGE (V TYP)	POWER DISSIPATION (mW TYP)[3]	COMMENTS
ANALOG DEVICES								
AD9685	2.2	—	20	±5	±2.5	+5/−5.2	210	ECL-COMPATIBLE
AD9687	2.7	—	20	±5	±2.5	+5/−5.2	430	ECL-COMPATIBLE, DUAL
ADVANCED MICRO DEVICES								
Am685-L (INDUSTRIAL)	5.3	—	10	±2	±3.3	+6/−5.2	300 MAX	ECL-COMPATIBLE
Am686C	9.0	—	10	±3	−3.3/+2.7	+5/−6	415 MAX	TTL-COMPATIBLE
Am687	7.0	—	10	±3	−3.3/+2.7	+5/−5.2	485 MAX	ECL-COMPATIBLE, DUAL
LH2311	200	200,000 TYP	0.25	±7.5	±13	±15	—	STROBED OUTPUT, DUAL
Am6685	2.5	—	15 TYP	±0.5 TYP	±3	+6/−5.2	180	ECL-COMPATIBLE
Am6687	2.5	—	15 TYP	±0.5 TYP	±3	+5/−5.2	360	ECL-COMPATIBLE, DUAL
FAIRCHILD								
μA711C	40	700	100	±5	±5 MIN	+12/−6	130	STROBED OUTPUT, DUAL
μA734C	200	35,000	0.05	±5	±10 MIN	±15	145 MAX	
μA760C	16	7000 TYP	60	±6	±5 TYP	±6.5	175	
HARRIS								
HA-4905	215 MAX	400,000 TYP	150	±7.5	±15	+5, ±15	190	QUAD; SINGLE-SUPPLY OPTION
HONEYWELL								
HCMP96870	2.0	—	20	±5	—	+5/−5.2	—	ECL-COMPATIBLE, DUAL
INTERSIL								
ICL8001C	250	15,000	0.25	±5	±10 MIN	+5/±15	30	LOW POWER; THIN-FILM RESISTORS
LeCROY								
MVL407	2.5	—	7.0	—	−2/+1.7	±5	420	ECL-COMPATIBLE, QUAD
LINEAR TECHNOLOGY								
LT1011AC	150	200,000	0.025	±0.5	−14.5/+13	±15	74	5V SUPPLY OPTION
LT1016C	10	1400	10	±3	−3.75/+3.5	±5	140	LATCHED OUTPUT; SINGLE-SUPPLY OPTION
LT1017C	1500	316,000	0.015	±1	—	1.15 TO 40	0.15	LOW-POWER DUAL
LT1040C	80k	—	0.3	±0.5	±5V	±5V	0.0025	CMOS SWITCHED-CAPACITOR DUAL
MOTOROLA								
MC1414	40	1000	25	±5	±5	+12/−6	230	STROBED OUTPUT, DUAL
NATIONAL SEMICONDUCTOR								
LF311	200	200,000 TYP	150 pA	±10	−13.5/+14	±15	138	FET-INPUT
LM319	80	8000	1.0	±8	±13	±15	165	DUAL
LM361	14	3000	10 TYP	±5	±5	+5/±10	250	±15V SUPPLY OPTION
LM393	1300	200,000	0.25	±5	0/+3	5	2	LOW-POWER DUAL, ±15V SUPPLY OPTION

Table continues on pg 50

The Latest Word in Gate Arrays:
Microtachyanorexilogopraxis

And a few words of explanation.

Raytheon introduces a family of advanced Oxide-Isolated bipolar gate arrays combining density, high speed, low power consumption, and Integrated Schottky Logic. The 5,040 gate, 150 I/O, CGA 50L15. The 3,584 gate, 124 I/O, CGA 35L12.

☐ **High performance:** 1.2nS, 160μW (typical) gate performance for <0.2pJ speed-power product. Selective enhancement to 1.0nS. (Runs twice as fast as CMOS, without severe loading degradation. And total chip dissipation <1.5W at top speed.) Full military performance, radiation hardness.

☐ **Flexible service and support:** complete integration of design and manufacturing eliminates gate array anxieties. Fully automated CAD (including conversion from logic simulation to placement and routing, linkage between logic simulator and tester). Flexible customer interface points, program manager support.

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REPRESENTATIVE VOLTAGE COMPARATORS *(Continued)*

MANUFACTURER AND MODEL[1]	RESPONSE TIME[2] (nSEC TYP)	VOLTAGE GAIN (V/mV MIN)[3]	INPUT BIAS CURRENT (μA MAX)[3]	INPUT OFFSET VOLTAGE (mV MAX)[3]	DIFFERENTIAL INPUT VOLTAGE (V MAX)	SUPPLY VOLTAGE (V TYP)	POWER DISSIPATION (mW TYP)[3]	COMMENTS
PLESSEY								
SP9685	2.5	250	20	±5	±2.5	+5/−5.2	292 MAX	ECL-COMPATIBLE
SP9687	2.5	250	20	±5	±2.5	+5/−5.2	584 MAX	ECL-COMPATIBLE, DUAL
PRECISION MONOLITHICS								
CMP-01E	110	200,000	0.6	±0.8	±12.5	±15	103	
CMP-02E	190	200,000	0.05	±0.8	±12.5	±15	99	LOW INPUT CURRENT
CMP-04FP	1300	70,000	0.2	±2.0	0/+3.5	+5	60	LOW-POWER QUAD; SINGLE-SUPPLY OPTION
CMP-05E	55	8000	1.2	±0.25	±3	±5	105	HIGH SPEED; LATCHED OUTPUT
RAYTHEON								
RC4805E	30	15,000 TYP	2.5 TYP	±0.8	±2	±5	140	HIGH SPEED; LATCHED OUTPUT
SIGNETICS								
NE521	8	—	40	±10	±3	±5	210	HIGH-SPEED DUAL; STROBED OUTPUT
NE527	16	—	4	±10	±5	+5/±10	250 MAX	COMPLEMENTARY STROBED OUTPUTS
NE529	12	—	50	±10	±5	+5/±10	250 MAX	COMPLEMENTARY STROBED OUTPUTS
SILICONIX								
L161C	5000	10,000	0.2	±6	−3/+1.3	±3	1.26	LOW-POWER QUAD; ±15V SUPPLY OPTION
TEXAS INSTRUMENTS								
TL510C	30	10,000	20	±3.5	±5	+12/−6	90	STROBED OUTPUT
TL331C	1300	200,000 TYP	0.25	±5	0/+3.5	+5	2.5	±15V SUPPLY OPTION, LOW POWER
TL506C	28	40,000 TYP	25	±5	±5	+12/−6	186	DUAL; STROBED OUTPUT
TLC372C	650	200,000 TYP	1 pA TYP	±10	0/+3.5	+5	1.0	CMOS, DUAL, LOW POWER
TLC374C	900	200,000 TYP	—	±10	0/+3.5	+5	2.0	CMOS, QUAD, LOW POWER
(SEE NOTE 4)								
LM311	200	40,000	0.25	±7.5	−14.5/+13	±15	138	
LM319	80	8000	1.0	±8	±13	±15	165	DUAL
LM339	1300	200,000 TYP	0.25	±5	0/+3.5	+5	4	LOW-POWER QUAD
LM393	1300	50,000	0.25	±5	0/+3.5	+5	2	LOW-POWER DUAL

NOTES:
1. COMPARATOR MODELS LISTED ARE COMMERCIAL-TEMPERATURE-RANGE VERSIONS (PARAMETERS SPECIFIED AT 25°C) UNLESS OTHERWISE INDICATED.
2. RESPONSE TIMES ARE BASED ON A 100-mV STEP WITH 5-mV OVERDRIVE.
3. UNLESS OTHERWISE SPECIFIED.
4. THESE MODELS ARE MANUFACTURED BY NATIONAL, TI, MOTOROLA, SIGNETICS, AND OTHERS.

need for latch-circuit hysteresis, which is used in some comparators to prevent oscillation in the linear region.

One step down in speed are the comparators whose major application is in successive-approximation A/D converters of hybrid construction. These comparator types do strenuous work; they need both high speed and high gain. Too much speed (bandwidth) or gain, however, will cause the comparator to oscillate as a consequence of the unavoidable parasitic capacitance between output and input. Because of this constraint, comparators limit the achievable resolution and conversion time for many successive-approximation A/D converters.

Still, a minimum value of gain is required to ensure that the comparator output will switch reliably in response to a small input overdrive. Equally important, the comparator output must complete this output transition in time to respond properly to the converter's next bit decision. In a 12-bit converter, for example, the comparator must perform satisfactorily with an overdrive of ½ LSB, and preferably with less than that. If ½ LSB=1.22 mV and the comparator's output must change by 2V, the necessary gain is 2÷0.00122, or about 1640 min. Unfortunately, few of the comparators that offer enough speed for competitive A/D-converter designs can guarantee this much gain.

In some cases, hybrid converter manufacturers solve the gain problem by adding a discrete voltage amplifier in front of the comparator chip. A voltage amplifier with a gain of 50 to 80 allows the use of LM311 and LM319 comparators that otherwise would be unsuitable for these applications.

Suitable for A/D converters

Precision Monolithics' CMP-05E precision comparator is among the few devices suitable for use in 12-bit A/D converters. It guarantees a voltage gain of 8000 and a 55-nsec propagation delay with 5-mV over-

STANDARDS UPDATE

FCC TELECOM RULES, PART 68

Clarification of the 2nd, 3rd and 4th Report and Order (Docket 81-216) was offered by Mr. Bill Von Alven of the FCC to attendees of the EIA/ITG Conference in Washington, DC. The November conference attracted over 150 persons from the telephone and related industries to a series of specialized talks and demonstrations focussed on telephone interconnect issues.

The 2nd Report and Order now allows the connection of digital Network Channel Terminating Equipment to the network, while at the same time requiring testing and registration as with analog devices.

The 3rd Report and Order cleared up a number of rules and most particularly changed the signal power and on-hook resistance limits under Part 68. The 4th Report and Order offered clarification on the standards for alarm dialers.

The premier public demonstration of a specialized Part 68 Workstation™ from Compliance Design Incorporated also highlighted the EIA/ITG. Attendees saw demonstrations of a single rack setup that incorporates all the equipment necessary to test to the electrical specification of Part 68.

The Workstation tests include: (1) hazardous voltages and currents, (2) signal power limitations, (3) balance, (4) impedance limitations, (5) billing protection, and (6) surge. By putting all this technology together in a single unit, Compliance Design has made testing to the Part 68 specification simpler and easier than with jury-rigged collections of equipment now used in many locations. Cost of the Part 68 Workstation is $49,950 (FOB Boxborough, MA) and includes complete documentation plus one full day of training. Circle the Compliance Design Reader Service Number below for more information.

FCC EMISSIONS RULES — COMPUTERS, PERIPHERALS, AND ELECTRONIC EQUIPMENT, PART 15

A complaint from Keytronics to the Federal Communications Commission has caused government action against a foreign manufacturer. Five retail outlets have been cited for handling Model 5151 keyboards made by the Taiwanese firm Behavior Communications. Keytronics complained that the keyboards did not have the proper FCC authorization and that Behavior Communications therefore had an unfair trade advantage.

As budgets are trimmed in Washington, investigation and enforcement rely more and more heavily upon tips and complaints like this. The Commission's resources are better spent in handling actual non-compliance cases than in routine cataloguing and rulemaking.

And attacking a manufacturer's or importer's distribution chain is one of the most effective remedies the Commission has in interdicting illegal equipment. Retailers, distributors, and even lessees and owners are liable for compliance with such regulations as FCC Part 15. Fines and possible imprisonment are effective deterrents to the sale of non-complying devices. There are several recent cases in which the FCC attacked distribution channels in an effort to stop the sale of non-complying devices.

ELECTROSTATIC DISCHARGE

Static problems sweep across the nation on the heels of cold, dry weather. Tied to this will be innumerable computer crashes resulting from electrostatic discharge (ESD). Though these failures are often misdiagnosed as line transients, the fact is that a variety of common occurrences as simple as a spark jumping from an operator's finger can be at fault.

Before a fatal data loss strikes your equipment, take steps to protect it and your customers from the hazards of ESD, advise the engineers at Dash, Straus & Goodhue, Inc. They can test, modify, and verify equipment as complying with industry and government standards.

An exclusive charge reservoir probe tip gives the Compliance Design ESD simulator a slew rate of up to 20,000 volts per nanosecond. It simulates the actual human-ESD event better than any other instrumentation, and allows engineers to test for ESD protection more accurately. For information on the simulator and ESD standards, contact Compliance Design.

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The leading reference book for compliance topics is now available free of charge to engineers, attorneys, and others with compliance responsibility. Topics covered include: FCC Part 15 and Part 68, CS-03 (Canadian, telecom interconnect), VDE (West German, emissions), and ESD. ***COMPLIANCE ENGINEERING 1985–1986*** is an expanded version of last year's first edition. It includes authoritative articles on design, test procedures, fixes, and legal rules and interpretations. To receive your copy at no charge, circle the Reader Service Number below.

All inquiries are handled in complete confidence.

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Dash Straus & Goodhue

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617-263-2662

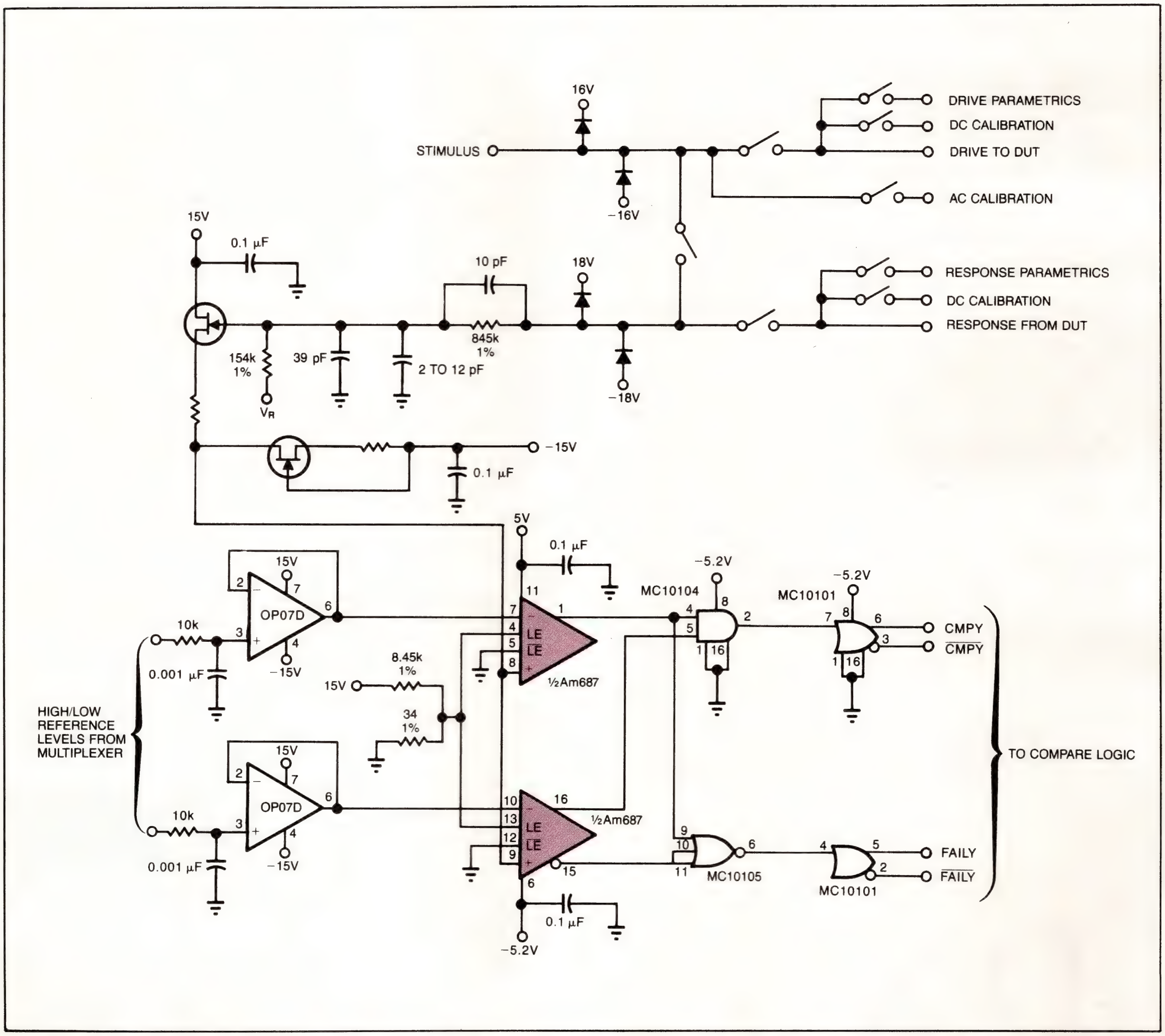
drive. PMI's zener-zapping trimming method reduces the input-offset voltage to 0.25 mV max. In addition, an output latch control allows you to make comparison decisions on a sampling basis.

Raytheon's Model RC4805E comparator is plug compatible with the CMP-05E. It specs a 30-nsec propagation delay but no guaranteed minimum gain (typical gain is 15,000). The device includes a latch for the TTL-compatible output. Linear Technology Corp's LT1011 offers 12-bit performance but requires an external latch for A/D-converter applications. This comparator specs a 250-nsec response time (150 nsec typ) and a gain of 200,000, guaranteed for a single 5V supply as well as bipolar supplies from ±5 to ±15V. All specs but gain are guaranteed over the operating temperature range.

Speed compromises accuracy

Several other comparators are fast and therefore worthy of mention, but you may find their high bias currents unattractive for use in A/D converters with better than 8-bit resolution. Signetics' 22-nsec max NE529, for example, specs a 50-μA input bias current; the 26-nsec NE527 reduces bias current to 4 μA by adding input emitter-followers to the input stage. The voltage gain is not specified for either product.

National Semiconductor's 20-nsec max LM361 and Fairchild's 16-nsec typ μA760C also require high bias currents. Their respective gain specs are 3000V/mV and 7000V/mV (the latter figure assumes the maximum allowed supply voltages). Both comparators provide complementary outputs. The LM361 includes an



An Am687 dual comparator senses voltage levels from a remote device under test in this digital option for LTX's LTX77 linear/digital IC tester.

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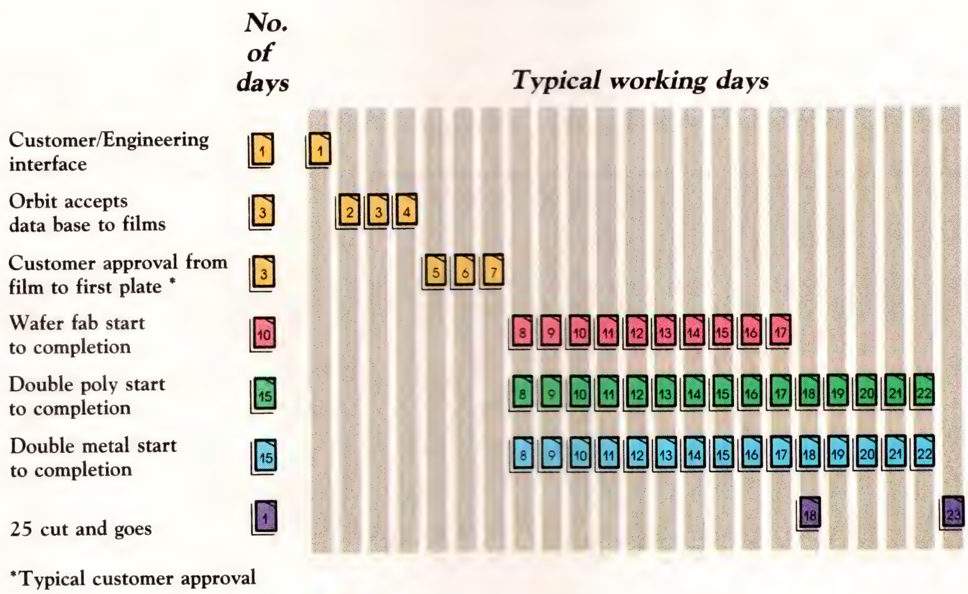

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CIRCLE NO 44

independent strobe for each output.

Not all comparator applications require high speeds. You probably wouldn't mind if a comparator took several microseconds to indicate a low battery voltage after it had monitored the battery for three weeks. The LT1040 from Linear Technology is suited to this and many other tasks requiring low power consumption. Based on a silicon-gate CMOS process and switched-capacitor circuit techniques, this dual sampling comparator draws only 1 nA while in the standby mode.

Unique circuit architecture

The LT1040 has little in common with more conventional comparators. Its A and B sections each have two pairs of differential inputs, and each comparator's output logic state follows the arithmetic sum (positive or negative) of voltages applied to its four input terminals. You can choose to sample these input voltages on command or to sample them at a rate set by an internal oscillator, with the frequency (0.1 Hz to 1 kHz) determined by an external resistor and capacitor. The comparator's response is completed 80 μsec after an external command or internal strobe, and it's independent of overdrive voltage.

Three additional outputs augment the LT1040's versatility. The pulsed-power terminal asserts the V^+ supply voltage for the duration of a comparison sample, letting you save power by activating an external circuit (a resistive bridge, for example) only when needed. The $\overline{(A+B)}$ output connects the comparator outputs in a NOR gate to simplify window-comparator hookups, and the on/off output is derived from on-chip logic that lets you implement bang-bang controller applications with few external components.

Other comparator types fit a variety of niche applications and offer a range of electrical performance—in part because many devices are simply old and represent a bygone state of the art. In addition to a selection of parameter values, these types offer low power consumption for remote and battery-powered systems, low-voltage (1V) supply operation, FET inputs to provide low bias currents, and output stages that simplify the interface to different logic families. Some types come in dual and quad versions to reduce the package count in a system.

CMOS technology offers the obvious way to achieve low power consumption. Texas Instruments' dual TLC372 and quad TLC374 comparators, based on the company's linear-CMOS process, draw only 0.1 mA per comparator from a 5V supply. However, Linear Technology's LT1017 is a bipolar dual-comparator IC that draws even less supply current—0.15 mA total from a 5V supply. Other low-power bipolar devices include the familiar LM393 dual comparator (0.4 mA) and the LM394 quad device (0.8 mA). Siliconix's L161 quad comparator, the TI TL331, and the Intersil ICL8001 also feature low current draw. (All these supply currents are measured under static conditions and with no output load.)

In addition, you can find comparators that operate with supply voltages as low as 1.15V or ±2V. The demand for these low-voltage comparators should escalate, along with the trend toward finer-geometry ICs that require low supply voltages

For more information . . .

For more information on the voltage comparators mentioned in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Advanced Micro Devices Inc
Box 3453
Sunnyvale, CA 94088
(408) 732-2400
Circle No 710

Analog Devices Inc
Two Technology Way
Norwood, MA 02062
(617) 329-4700
Circle No 711

Fairchild Camera and Instrument Co
3333 Bowers Ave
Santa Clara, CA 95051
(408) 987-9530
Circle No 712

Harris Semiconductor Corp
Analog Div
Box 883
Melbourne, FL 32901
(305) 724-7000
Circle No 713

Honeywell Inc
Signal Processing Technologies
1150 E Cheyenne Mountain Blvd
Colorado Springs, CO 80906
(303) 576-3300
Circle No 714

Intersil Inc
10710 N Tantau Ave
Cupertino, CA 95014
(408) 996-5000
Circle No 715

LeCroy Research Systems Corp
700 S Main St
Spring Valley, NY 10977
(914) 425-2000
Circle No 716

Linear Technology Corp
1630 McCarthy Blvd
Milpitas, CA 95035
(408) 942-0810
Circle No 717

Motorola Semiconductor Products Inc
Box 20912
Phoenix, AZ 85036
(602) 244-6900
Circle No 718

National Semiconductor Corp
2900 Semiconductor Dr
Santa Clara, CA 05051
(408) 737-5000
Circle No 719

Plessey Semiconductors Inc
3 Whatney
Irvine, CA 92718
(714) 951-5212
Circle No 720

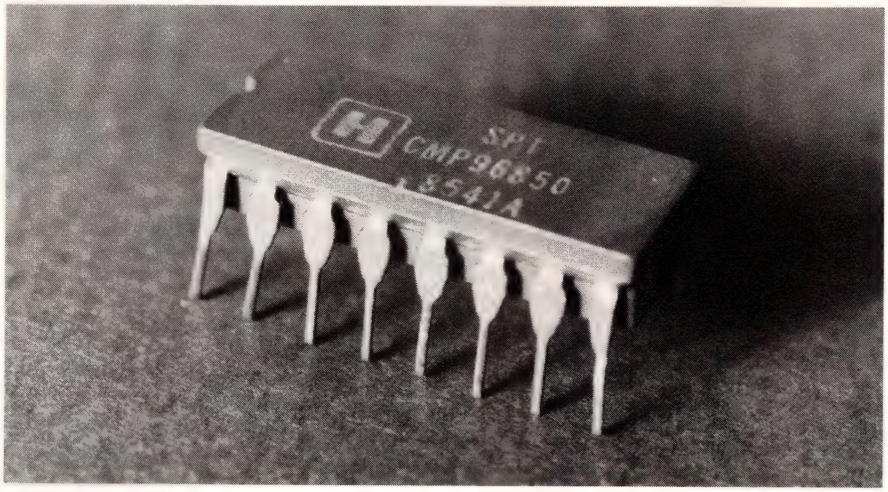
Precision Monolithics Inc
1500 Space Park Dr
Santa Clara, CA 95050
(408) 727-9222
Circle No 721

Raytheon Co
Semiconductor Div
350 Ellis St
Mountain View, CA 94043
(415) 968-9211
Circle No 722

Signetics Corp
Box 3409
Sunnyvale, CA 94088
(408) 739-7700
Circle No 723

Siliconix Inc
2201 Laurelwood Rd
Santa Clara, CA 95054
(408) 988-8000
Circle No 724

Texas Instruments
Semiconductor Group
Box 225012
Dallas, TX 75265
(214) 995-2011
Circle No 725



***The HCMP96850 high-speed comparator** from Honeywell is suitable for use in automatic test equipment and high-speed instrumentation. Propagation delay is less than 3 nsec.*

(Ref 2). Currently available low-voltage comparators include Linear Technology's LT1017 and LT1040C, Siliconix's L161, and the generic LM339 and LM393.

National Semiconductor's LF311 FET-input comparator provides subnanoampere input bias currents that almost eliminate bias-current errors. The device can operate from a single 5V supply or from ±15V supplies. Its ±10-mV max input offset voltage rules out some applications, however.

Commodity-comparator products like the quad LM339 are popular, principally because of their price: You can buy the LM339 for about $0.35. "At that price they are virtually free," says Phil Perkins, chief engineer, advanced development for LTX Corp. It's also easy to design parts like the LM339 into the applications for which they're best suited.

Still, Perkins would be willing to pay considerably more for an enhanced LM339. The part's output swings to the negative power-supply rail, for example, so with bipolar supplies you often must add a level translator to make the output compatible with the load circuit's logic requirements. A 16-pin package and a logic-level select pin controlling all four of the comparator outputs would address this problem. Also, Perkins suggests, it would be nice to have a middle-performance comparator that specs a 100-nsec response time and a decent common-mode range but is easy to apply like the LM339. Lower input bias current would be welcome, so the device might profit from FET inputs.

Improvements in voltage comparators need not depend entirely on improved technology. A better dialogue between the makers and users could lead to models with a more useful combination of the features that are already available. One technology development seems certain, however: the use of gallium arsenide to speed the performance of linear ICs. Within the year you may see GaAs voltage comparators that feature 0.5- to 1.0-nsec propagation delays, gains of 200, and input bias currents below 20 nA.

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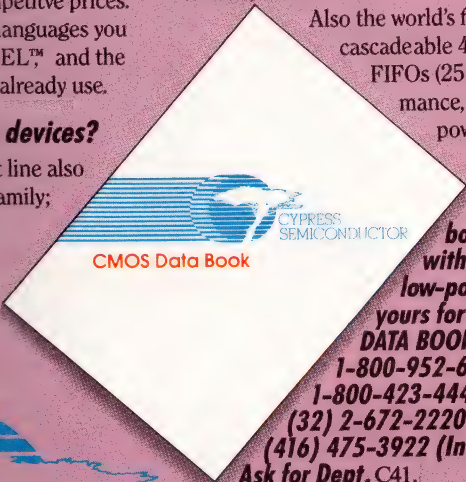

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Logic analyzers evolve in response to high-level languages

Charles H Small,
Associate Editor

In parallel with the design engineer's journey from pencil-and-paper designs and discrete parts to high-level languages and programmable ICs, logic analyzers—in their latest incarnation as software analyzers—have also evolved by becoming high-level-language instruments. Although the software analyzer is a logical and necessary extension of the concept of logic analysis into the realm of high-level software, the instruments are so new that not even their makers, let alone software engineers, fully appreciate all the changes that the instruments will wreak on software-engineering methods.

From their introduction, logic analyzers gave engineers a new way of looking at phenomena—seeing events in parallel instead of serially. Software analyzers, similarly, provide new ways of analyzing software and viewing the phenomena associated with the software under development (see **box,** "From logic to software analyzers"). In addition, hardware-based software-performance analyzers prove useful earlier in the software-design cycle **(Fig 1)** than do software-based analyzers (program profilers).

Typically, hardware-based software analyzers make five classes of measurements on program statements and data constructs:

- Intermodule linkage
- Program activity
- Memory activity
- Module duration
- Module usage.

That is, the analyzers can record extended sequences of subroutine or procedure calls, the frequency of

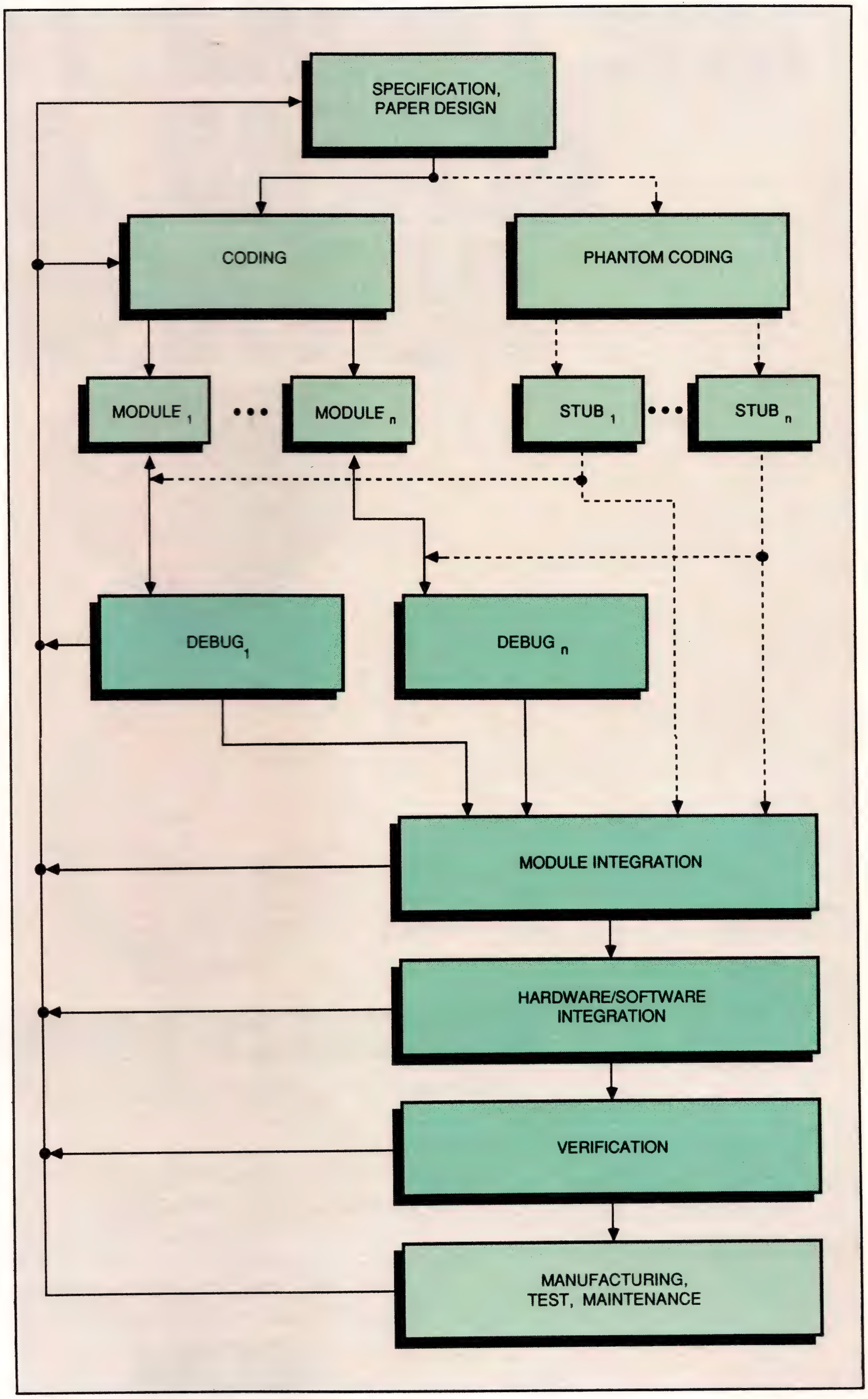

*Fig 1—**You can use hardware-based software-performance analyzers** early in the software-design cycle. Unlike software-based analysis tools, which typically wait until the verification stage, hardware-based tools prove useful as soon as you need to debug multiple modules.*

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From logic to software analyzers

Early logic analyzers served low-level-logic designers by capturing multiple channels of timing data and displaying them in fundamental terms—timing diagrams. Although logic analyzers never lost the capability to display timing waveforms, the instruments gradually acquired additional abilities in response to design engineers' changing needs. Logic analyzers could soon capture, format, and display data in forms increasingly abstracted from the electrical activity in the circuits under test. The first step along the road to handling high-level languages was the state analyzer. State analyzers compress captured data into lists of numbers or characters—usually binary, octal, hexadecimal, or ASCII.

Analyzers become abstract

Next, state analyzers became μP analyzers when they acquired μP-specific interfaces and the ability to disassemble captured data into the assembly-language mnemonics of the targeted μP. Inferring the assembly-language program from captured data is a relatively simple process because of the one-for-one correspondence between an assembly-language instruction and the corresponding μP state that the analyzer sees at the μP's pins. Further, μP analyzers that are integrated into a hardware/software development system can easily consult the assembler's original symbol tables and plug labels back into a disassembled listing in place of raw hexadecimal numbers where appropriate. Thus, although the term "software analyzer" refers to high-level-language instruments and doesn't refer to μP analyzers, the μP analyzers are really a rudimentary kind of software analyzer.

High-level software analyzers are just now beginning to appear. These instruments attempt a much more difficult task than μP analyzers; a software analyzer's job is to trace high-level-language execution and data constructs based on observations of a μP's address, data, and status lines. Decompiling machine-level activity into high-level code is much more difficult than disassembling because no one-for-one correspondence exists between a high-level-language construct and the code it becomes through compilation—particularly if you invoke the compiler's optimizing option. The degree of abstraction of high-level languages from the μP's activity is high, and no clear-cut path exists between the two domains.

In fact, software analyzers don't really decompile captured data. Instead, they rely on myriad clues to associate certain kinds of μP activity in specified memory areas with a corresponding section of a high-level program. Therefore, software analyzers cannot function without extensive cross-reference information from the compiler that generated the object code that the instrument is analyzing. The software analyzer must know, for example, not only the absolute locations of all variables and other data constructs of interest, but also the mechanisms the compiler uses to pass variables between modules or subroutines and the locations of all specified program modules' entry and exit points.

Armed with this cross-reference information and understanding the compiler's mechanisms, the software analyzer can correlate your high-level debugging commands with the low-level activity it sees at the μP's pins. Moreover, after capturing data, the analyzers can condense and display them in ways that help you pinpoint program bugs.

program flow to selected parts of the code, the program's destination in memory, length of run time for selected modules, and frequency of calls for selected modules. You specify all of these program and memory areas using the same terms used in your original source code. The analyzer then correlates those commands with the correponding object-code and memory areas and configures itself to trigger on low-level events.

Somewhat confusingly, three types of software analyzers currently exist. Real-time software analyzers (also called software-performance analyzers) have specialized, fast hardware that allows them to obtain one-shot timing data. Nonreal-time analyzers, on the other hand, must occasionally interrupt the software under test to record the state of program constructs or the μP because they lack fast hardware. Finally, some so-called software analyzers mimic conventional software-based program profilers. Like the software tools they mimic, these analyzers measure repeated runs of the same program to gather and reduce statistical data. Consequently, they prove useful only during the final-verification stages of software development.

The key difference between the hardware- and software-based methods of software analysis is that in using the latter method, you must instrument your program; with the former method, you instrument the hardware (see **box,** "Software- vs hardware-based tools"). Thus, users of software-based software analyzers must edit and recompile their programs each time they change their measurement setups. Hard-

Software- vs hardware-based tools

Because the advocates of software-based software analyzers have experience only with program profilers, they consider only module duration and module usage to be software-performance analysis. To them, software analysis is a tool to be applied only during the last phases of a software project for what they loosely term "optimization" ("fine tuning" is in fact a more apt term). By optimization, they mean that after measuring the time consumed by various program modules, they rewrite the slowest and most frequently called ones so that those modules execute faster, thereby speeding the overall program's execution. (They can also, at this juncture, eliminate the phantom modules that are never called. Such phantoms seem to lurk, needlessly occuping memory, in every large program.)

Application area expands

But this myopic view of software analysis overlooks the utility of the new hardware-based software analyzers early in a software-design project. Conventional software-based software-analysis tools are too cumbersome to be applied economically anywhere other than during the final phases of a project. In contrast, hardware-based software analyzers are much faster to set up and run. Therefore you can use hardware-based software analyzers to trace module-to-module jumps and to trace variables passed between modules early in the software-design cycle—in fact, as soon as you have just two modules to check. In other words, software analyzers' area of application isn't limited to just conventional software analysis; it also overlaps what conventional wisdom considers debugging.

A typical debug session

The software analyzers' abilities begin to make sense when you consider how you might perform a typical high-level-language debugging session with the aid of a hardware-based software analyzer. Recall that the conventional software-based debugging tools generally allow only single-stepping through modules line by line, module by module; you then manually examine the program's state. This debugging scheme is laborious and far from optimal because it begins with the particular instead of the general.

A hardware-based software analyzer, on the other hand, allows you to start at the highest, most abstract level of your program's algorithm: how the program's modules interact. You can use the software analyzers' module-linkage tracing facility to see if the sequence of modules is according to your plan.

From general to particular

If the sequence of modules proves correct, you could next trace common (global) or shared data constructs (data passed between modules) in an effort to find data being corrupted. Once you've homed in on the offending module, you could then dip into that module's execution to trace its local variables. When you find a local variable with wrong data, then (and only then) you can revert to conventional software-debugging practice and trace your program line by line.

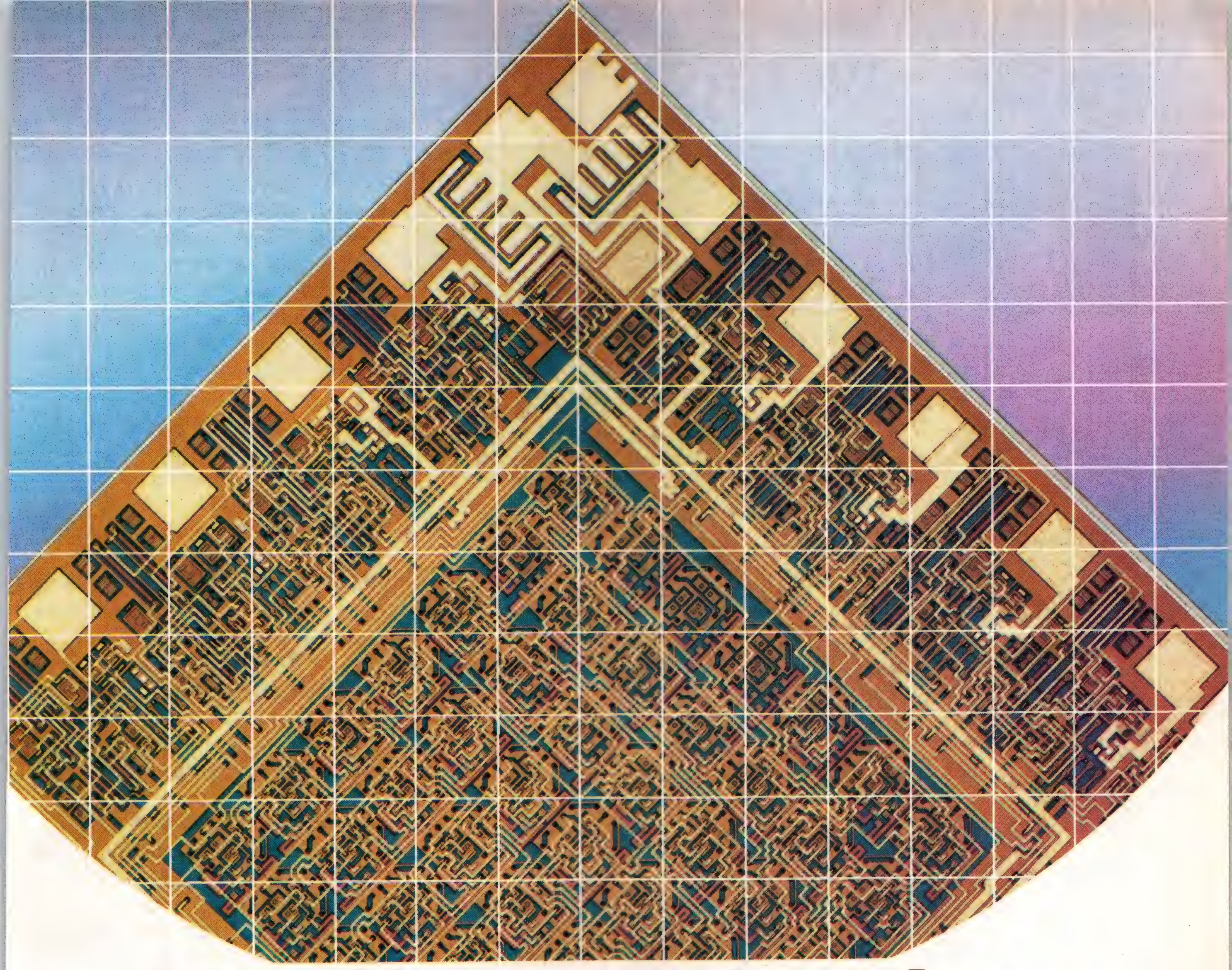
Proponents of software-based software analyzers might argue that they could duplicate this sequence of descending from module linkages to statements by peppering their programs with Print statements at appropriate locations. They could determine module entry and exit points by inserting commands to print such announcements as "entering module A" and "exiting module A" at the beginning and end of module A's statements. Similarly, they could print the contents of various data constructs at key points in the program.

Although the software-based analyzer proponents *could* thus duplicate some of a hardware-based software analyzer's abilities, experience shows that the software method is too time consuming and its output too difficult to interpret; in addition to making real-time measurements that software methods can't hope to duplicate, the hardware-based software analyzer is easier to use, and its output is easier to interpret.

ware-based software-analyzer users, on the other hand, can run the same program over and over without time-consuming recompilation because they don't depend on in-line code. Each user will have to decide whether his or her time is valuable enough to warrant the $3000 to $11,000 (depending on model) for a hardware-based software analyzer.

Paying the price

Not all hardware-based tools are that easy to use, however, and not all have wide application areas. Of the major logic-analyzer makers, all offer some form of software-performance analysis in their state analyzers. And all complain that users neither appreciate nor understand the feature. However, a software analyzer that has a limited range and that must be programmed manually (each time you change just one routine and recompile and relink, all the absolute addresses change and



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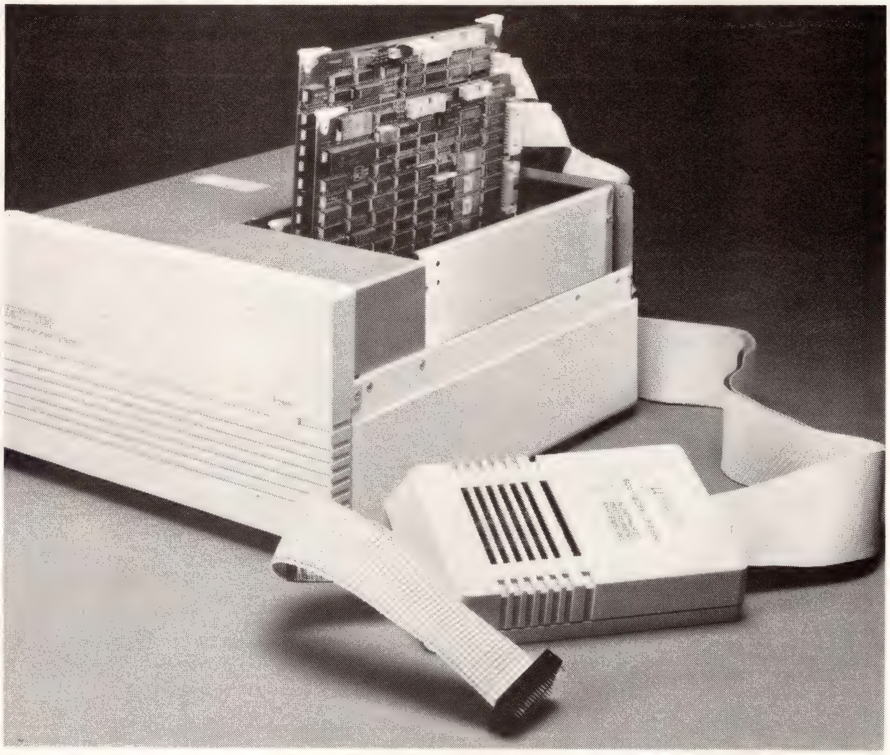

Specialized for gathering software data, Northwest Instrument Systems' Softanalyst times program execution, locates possible bottlenecks, and notes which routines are called frequently.

therefore must be updated) is likely to be used only when absolutely necessary. By excluding such limited devices, you're left with software analyzers that can both access a compiler's symbol tables and automatically access program hooks.

Real-time analyzer

The Hewlett-Packard HP 64340A software analyzer, for example, solves otherwise intractable problems of tracing the real-time execution of high-level programs. The $11,000 analyzer is a 3-board set for the company's HP 64000 μP development system (processor-specific analysis software costs $1000). In addition to the 64340A, a reasonably configured 64000 system will cost $20,000 or more.

Unlike the 64340A, other analyzers are befuddled by certain aspects of such high-level languages as Pascal and C because programs generated by these languages' compilers define certain variables and other data constructs as the programs run. Instead of preallocating to each data construct its own private memory area at compile time, the programs typically use and reuse a common area of memory—called a stack or heap—for data constructs. Therefore, you don't know where a given data construct will reside. Worse, a given memory location could successively contain several variables during different phases of a program's execution.

Because you must explicitly arm the event recognizers (address, data, and qualifier comparators) of other instruments before a program's test run, those instruments cannot handle dynamically declared data constructs in real time. Instead, they must inject pauses into the program's flow while the instrument takes a snapshot of the target system before resuming execution (that is, it moves a copy of the state of the data construct and the processor into data-capture memory).

The HP 64340A, however, can follow the execution of a program by using a combination of cross-reference data from the manufacturer's Pascal and C compilers, special hardware, and post-capture data reduction. The company is trying to convince other compiler suppliers to provide the necessary hooks with their compilers so that the HP 64340A will be able to work with compilers other than those supplied by Hewlett-Packard.

Family resemblance

Fig 2 shows the 64340A's architecture. The instrument's front end resembles that of a logic analyzer. The analyzer's inputs are in parallel with the inputs of the 64000's in-circuit emulator—that is, the analyzer sees the target μP's address, data, and status lines. The analyzer has an onboard 68000 μP and a 4k×96-bit data-acquisition memory. An acquisition-memory location stores not only the state of the μP—address, data, and status lines—but also a time tag, a computed program-counter value, and flags from the analyzer's state machines. The analyzer needs all this information for post processing.

Information that the analyzer gleans from the compiler allows the analyzer to set up its static and dynamic event recognizers. During a program's test run, the recognizers strobe data into the acquisition memory. After the test run, the 64000 system uses the information stored in the analyzer's acquisition memory to reconstruct the program's activity.

Tracing local variables

For example, suppose you want to trace one procedure's reads and writes to a dynamically defined variable that is local to that procedure. From the compiler's cross-reference tables, the analyzer knows the location of the beginning and end of the procedure's instructions and also knows how the compiler handles the procedure-entry overhead of setting up the local variables on the stack (the reserved area on the stack is called a frame). Further, the cross-reference data also gives the

64340A the position of a given variable—or offset—within the frame.

The analyzer arms its low-level recognizers with the procedure's entry and stack-setup instruction addresses. When it senses that the program has jumped to the procedure of interest and has set up its local variables, the analyzer calculates the absolute address on the stack of the variable by using both the current stack pointer (SP) and the known offset of the variable within the frame. The analyzer also sets up its Boolean-function generator. When the Boolean-function generator recognizes an access to the dynamically defined variable of interest, the analyzer records the 96-bit-wide state of the system under test. When the program's flow exits from the procedure, the analyzer dismantles the dynamic word recognizers' and Boolean-function generator's setup.

Because the analyzer's event recognizers can work in pairs, the analyzer can record activity over a range of addresses as well as at one address. The 64340A has enough event recognizers to monitor four ranges simultaneously. In this way, it can capture as many as 256 copies of a complete stack frame or other data construct as the program executes. You can also set up the pairs of event recognizers to trace your program's flow by procedure or by groups of procedures if the pairs of recognizers span entire procedures or groups of procedures. (You can trace groups of procedures only if the compiler has loaded the groups contiguously.)

The HP 64340A also traces statements and data constructs in nonreal time, as other analyzers do, by cross-triggering the development system's in-circuit emulator and by breaking execution when it sees hardware breakpoints. (A hardware breakpoint comes from an event recognizer; a software breakpoint comes from extra debugging instructions inserted at key points in the program.) The analyzer has nine hardware breakpoints that operate in parallel.

Further, the analyzer's remaining functional blocks allow it to count the number of occurrences of 255 different events. This real-time, nonintrusive ability proves useful—as does the analyzer's ability to measure the time the program spends in various procedures (time-stamp data)—in identifying procedures that run often or consume excessive amounts of computer time.

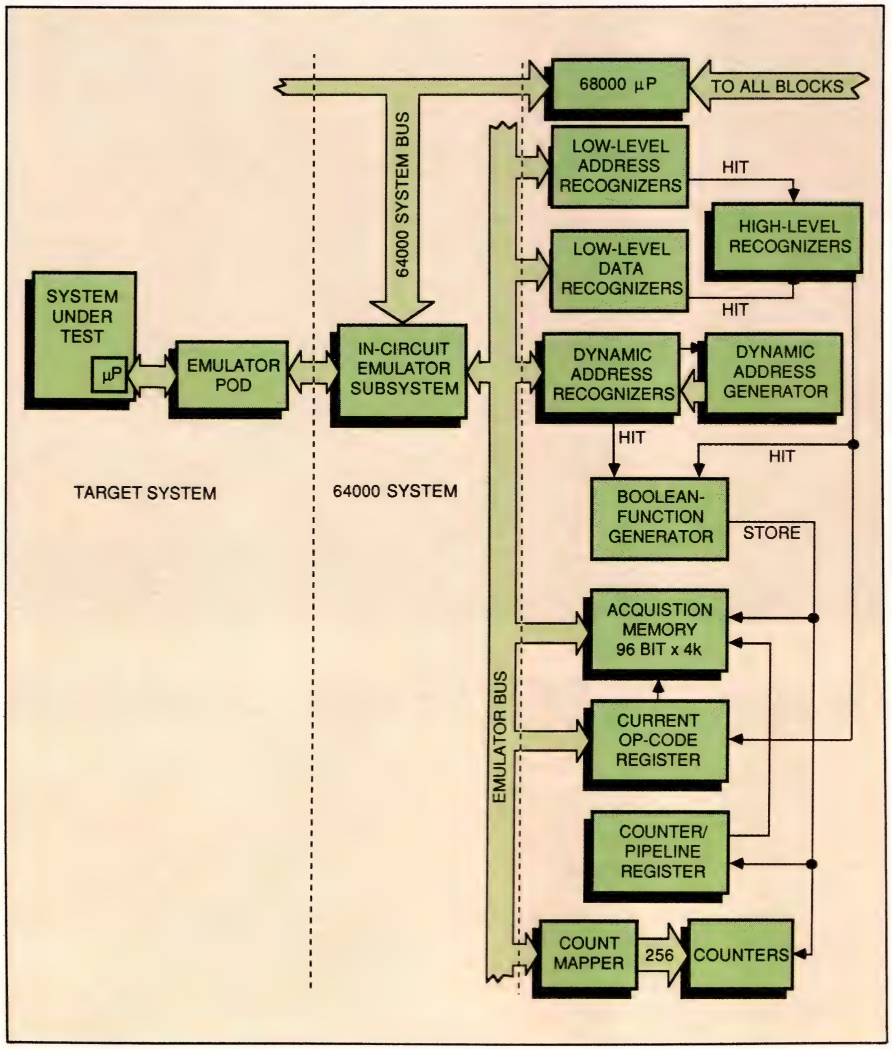

Fig 2—By using details gleaned from a high-level language's cross-reference tables, the $11,000 HP 64340A real-time software-performance analyzer can trace program activity in real time without injecting wait states into the target system's execution of the program under test.

Nonreal-time analyzer

If you can forgo real-time measurements, the $3000 HP 64330 provides a suite of measurements similar to that of the 64340. The low-cost instrument, however, cannot dynamically re-arm its event recognizers. Instead, it interrupts the emulator's processor when it needs to determine what the processor is doing. So although it can handle dynamically defined (as well as statically defined) program constructs, it cannot run in real time.

Hewlett-Packard also has a pair of software-performance analyzers—the $3440 HP 64310A and the $4350 to $9610 (depending on number of channels) HP 64620S—that provide only global measurements of module-execution times. These instruments fulfill classical software-performance roles and are un-

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suitable for the early phases of software development.

In contrast to the HP 64340, the front end of Northwest Instrument Systems' Softanalyst **(Fig 3)** looks nothing like that of a logic-state analyzer. Logic-state analyzers typically have no more than four high-speed comparators (or word recognizers). These comparators look for a match between your preprogrammed trigger event and the state of the system; they can't wait for more than four events at one time. However, you'd need far more than four word recognizers to cover all the branches, accesses, and events you'd be concerned with when analyzing a large structured program.

Softanalyst employs a 256-event-deep RAM array as an event recognizer. You can program the instrument to look for either 250 single events (such as the access of a variable) or 125 pairs of events (such as the entry to and exit from a software module or subroutine), or you can program it to monitor 83 address ranges (to investigate, for instance, access to an array or other data structure). When the instrument sees a trigger event, it records not only the event, but also a time tag for that event.

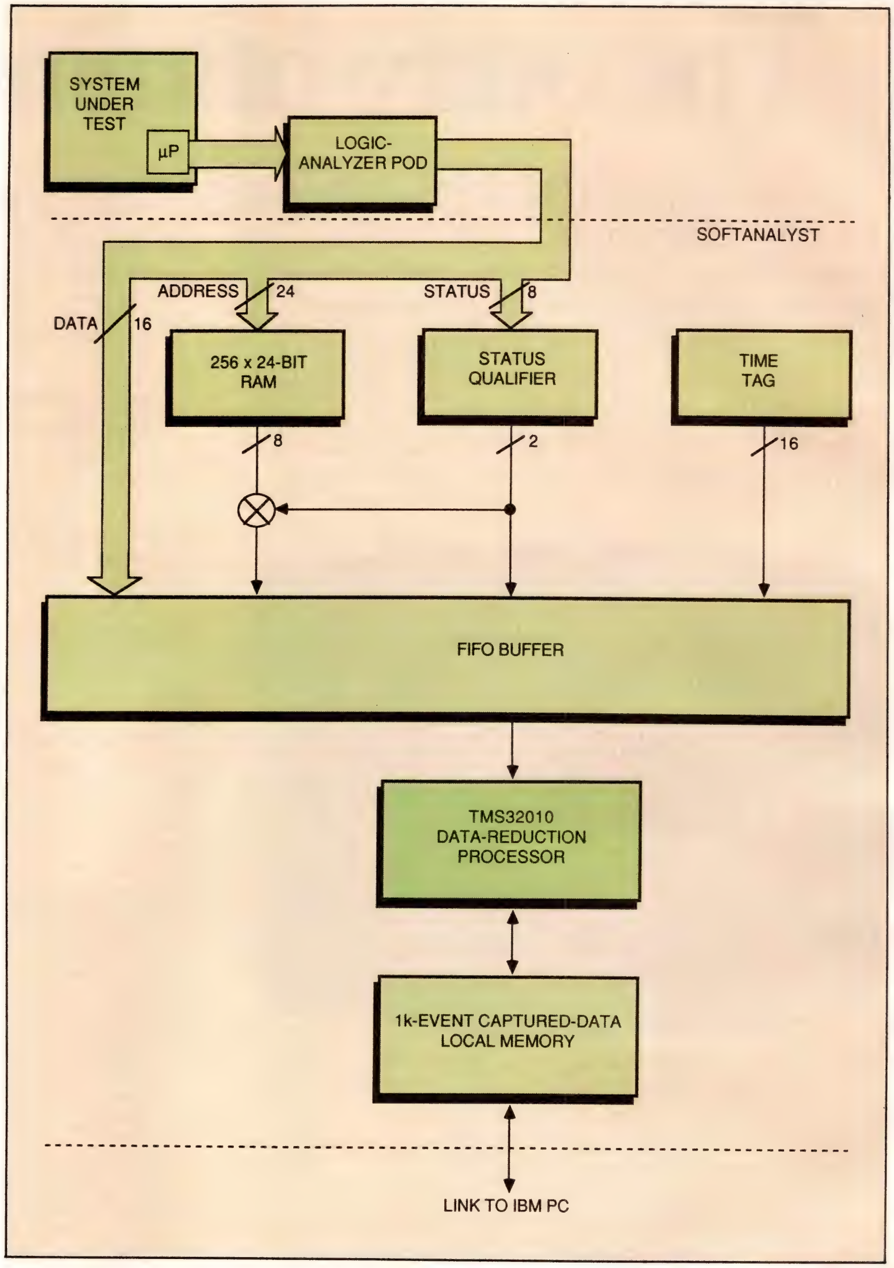

***Fig 3—A TMS32010 digital signal-processing µP** reduces and compresses data, thereby allowing the Northwest Instrument Systems' Softanalyst to monitor long program runs without overrunning its captured-data buffer.*

Real-time data reduction

Fig 3 also shows a key feature of the Softanalyst's architecture: the event recognizer's output goes into a FIFO buffer; the output of the FIFO buffer goes to a TMS32010 µP. Unlike analyzers that capture data until their capture memory is full and then reduce the data, the Softanalyst's TMS32010 continually reduces and compresses incoming data. This continual reduction means that (as long as the FIFO buffer doesn't overflow) the Softanalyst can capture data over longer periods than its 1k-event capture memory might at first suggest.

Unlike HP's software analyzers, the Softanalyst isn't integrated with the manufacturer's compilers. At present, Northwest Instrument's software analyzer accepts compilers' symbol tables in Intel object-module format (OMF) and in Unix-defined common object-file format (COFF). Once you've downloaded a symbol-table file to the software analyzer, you use a built-in windowing editor to select trigger events corresponding to lines of code, procedure entry and exit points, and data structures. Unfortunately, you'll have to repeat this downloading step each time you modify and recompile your program.

Besides simply recording the execution history of a module, the software analyzer can correlate the module's execution to the state of a system variable or the value of passed parameters at the time the module executes. In addition to collecting data on program activity,

the software analyzer can let you see the range of values that your program's variables assume during the program's run.

Measure variable's range

Softanalyst's minimum acquisition interval is 100 nsec, and its front end handles 24 address lines, 16 data lines, and eight status lines. At the fastest acquisition rate, the time-tag counter overflows in approximately four minutes; at the slowest rate, it runs for more than seven hours. The instrument works with predefined software constructs, so it can't trace dynamically defined variables. And because it sees only the μP's activity, it can't follow the activity of such independent hardware devices as memory-management circuits or satellite processors.

The Softanalyst requires an IBM PC or PC/AT for control. Including a mainframe, pc boards, an IBM PC interface board, and IBM PC software, the system costs $9200. A required μP-specific interface pod costs an additional $765 for the 68000 version and $1995 for the 8086/186 versions. **EDN**

For more information . . .

For more information on the software analyzers described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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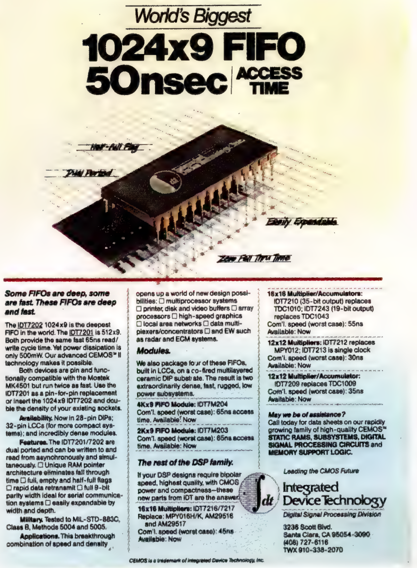

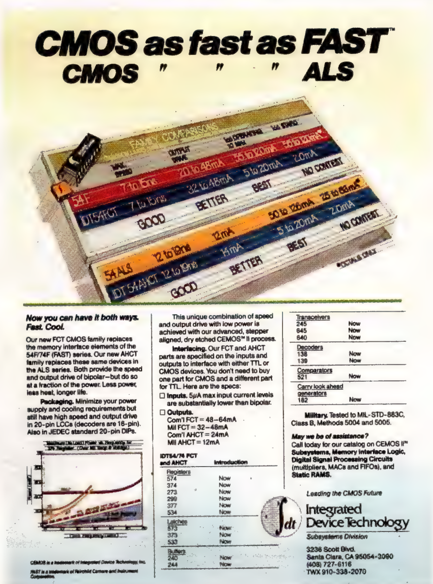

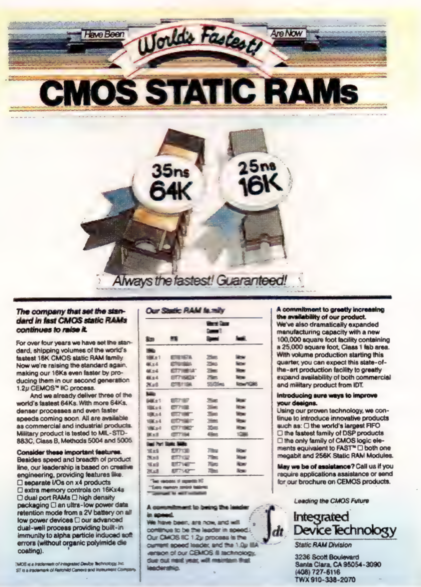

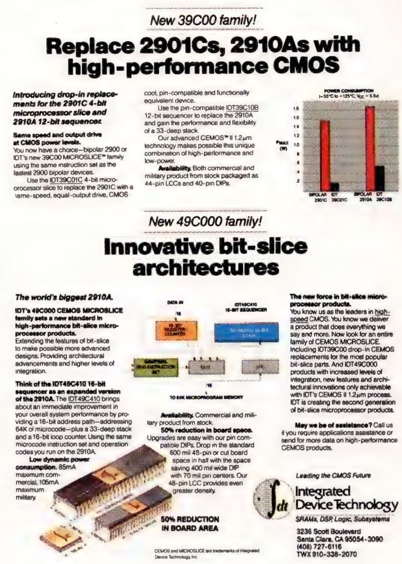

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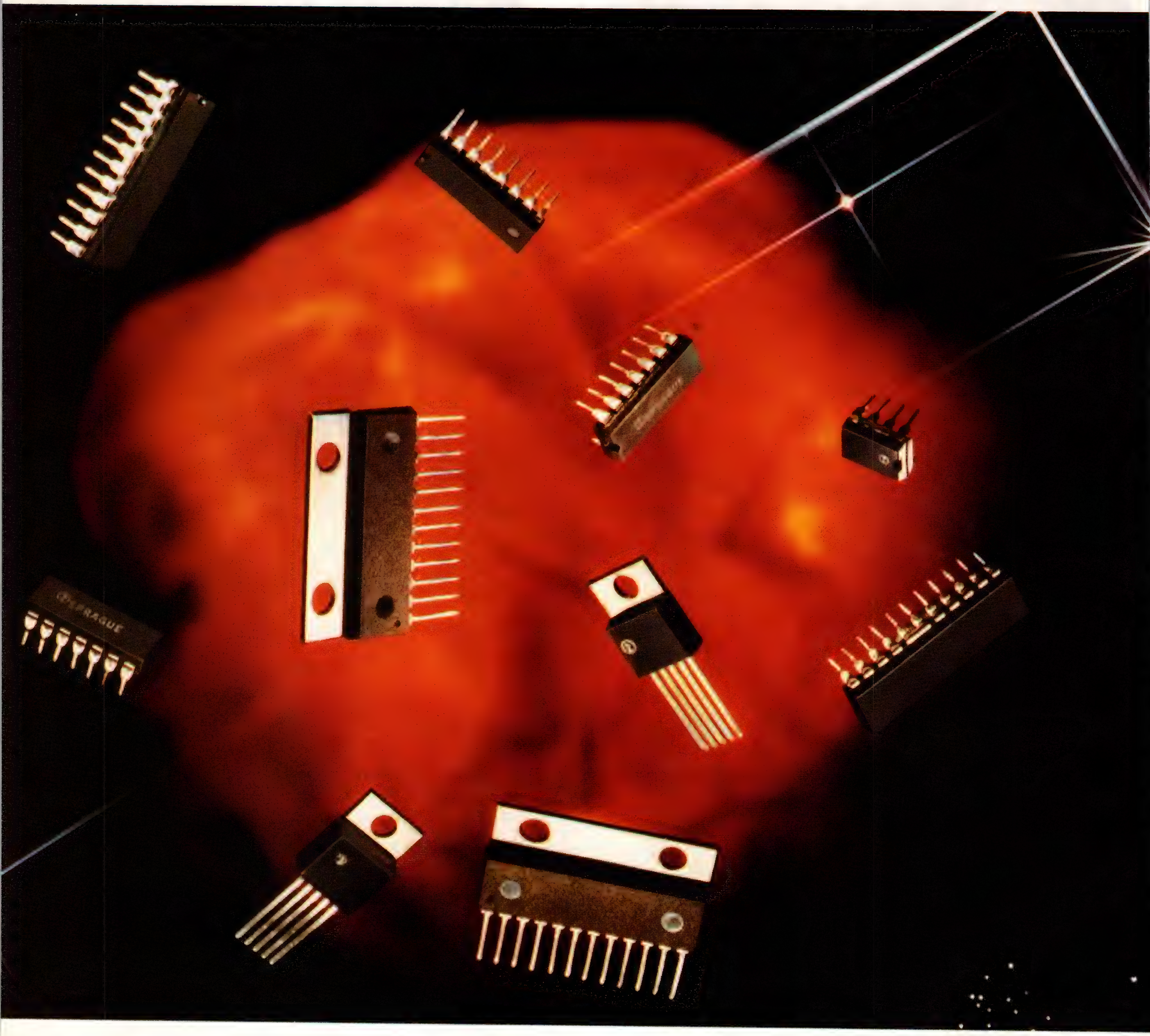

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CIRCLE NO 58

ISSCC '86 speakers predict future developments in solid-state technology

Robert H Cushman,
Special Features Editor

Designers who want authoritative forecasts of future trends in solid-state technology won't want to miss this year's International Solid State Circuits Conference (ISSCC), which will take place in Anaheim, CA (see **box,** "ISSCC registration details"). The conference will provide a forum for industry experts to speculate about technological developments that you can expect to see in the near future.

For example, the informal panel discussion "Microprocessors in the year 2001" will bring together such experts as John Slager of Intel (Santa Clara, CA), who heads the logic-design group for his company's 80386 (which is now engendering the 80486), and Frederico Faggin, who participated in such key historical projects as the initial 4040, 8008, and 8080 µPs at Intel, and then went on to create the Z80 at Zilog (Campbell, CA).

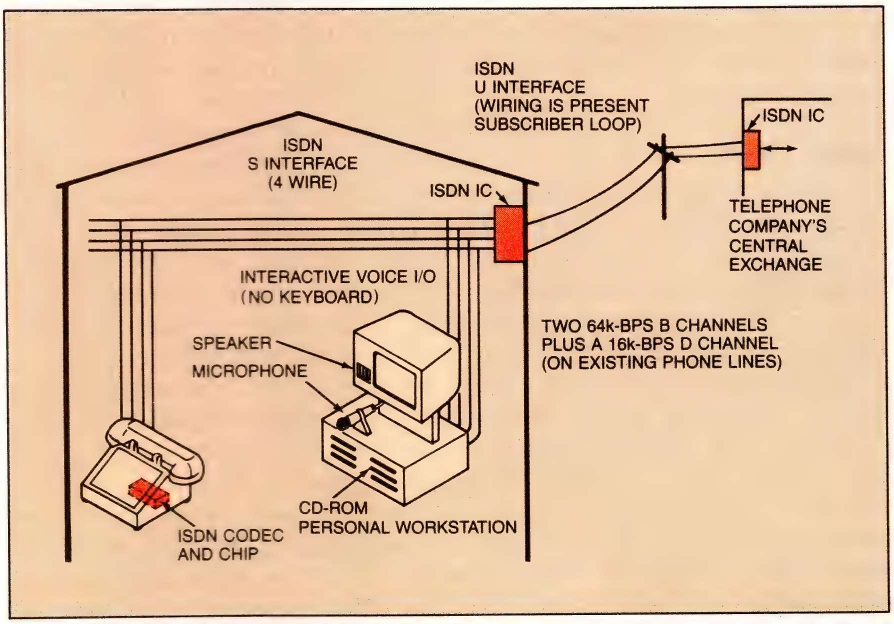
Slager, the panel organizer, believes that although current µP families such as the 80386 and 80486 will continue to develop, a radically new approach to microprocessors will emerge between now and 2001. He predicts that this new approach will make programming so easy that the industry will abandon established, software-entrenched µP families like the 8086/80386.

Faggin agrees, saying that it's unlikely that present µP families like the Z80, 8086, and 68000 will face much competition before 2001. Both Slager and Faggin are convinced that ease of use will be as important in new computer systems as raw performance is. Slager expects to see implementations of artificial intelligence in these systems, and Faggin predicts that these systems will begin to emulate the human brain.

Speakers and panelists at the conference will describe at least two relatively new types of µP architectures: the reduced-instruction-set computer (RISC) and the massively parallel architecture. This year, a number of actual examples of these architectures are appearing; they're no longer simply industrial and academic research projects.

According to Randy Katz, organizer and moderator of the Thursday evening panel discussion "Reduced instruction set computers: A new microprocessor era," serious debate over the merits of RISC vs CISC (complex-instruction-set computers) must take place, because a number of real RISC machines now exist. He cites the IBM 801 ROMP, HP's Spectrum, the MIPS from MIPS Inc, Inmos's Transputer, and the Fairchild Clipper as examples of real RISC machines. Panelists at this discussion will include both advocates and critics of RISC machines.

The other new architecture that ISSCC participants will consider, the massively parallel architecture, will provide a way to achieve higher µP performance: A massively parallel machine need not be especially fast to achieve high computation rates. The paper "A dynamically reconfigurable processor array chip" (**session 18**) suggests one practical way to achieve such an architecture. As one



***The personal workstation of the future** will be so user friendly that the human operator won't need a keyboard, say panelists at the ISSCC '86 informal discussion session "Microprocessors in 2001." The user will simply speak to the computer, which will interpret the commands via artificial-intelligence software. The personal workstation will provide as much power as mainframe computers currently do. In addition, the workstation's massively parallel array processor and cryogenically cooled accelerators will let it execute artificial intelligence software in real time. The ISDN telephone will have features like user-selected routing, including broadcast, and optional encryption. The system would give the user economical, effortless access to vast amounts of information, both locally (through devices like CD-ROMs) and globally (through the ISDN).*

of the authors, Steven G Morton of ITT, explains, you use the reconfigurability of the processor array to select good 1-bit slice processors on very large (500×600-mil) chips. Despite the chip size, Morton claims, you obtain acceptable yields (25%), because you put down more 1-bit-wide ALU slices on the die than you need; that is, where you need 16 bit-wide ALU slices, you put down 20.

At run time, the software selects 16 good ALU slices; any remaining good slices are reserves. The 16 slices make up a 16-bit-wide ALU. To make the massively parallel arrays, you wire large numbers of these 16-bit-wide chips into networks of rows and columns.

In a typical application, one program-control unit would send the same instruction to all the chips, which would then execute the instruction simultaneously. For algorithms that can be paralleled, the computation rate would increase accordingly. According to Morton, 200 of these chips could achieve a speed of 2 billion instructions per second (BIPS), despite the modest 10- to 12-MHz clock rates.

Cooled CMOS

A more direct way of obtaining increased performance for all CMOS architectures is to cool them cryogenically to very low temperatures (−196°C), as panelists at the Thursday evening discussion "Liquid-nitrogen-cooled CMOS" will suggest. According to one of the panelists, ETA Systems (St Paul, MN) will introduce a cooled-CMOS computer in 1986. This machine is a supercomputer that runs at 5M flops when cooled by air and 10M flops when cooled by liquid nitrogen. The machine uses semicustom CMOS circuits. Only the multiple CPUs are cooled.

The cooled-CMOS technique does involve some tradeoffs, however. Although it makes circuits faster by decreasing some of the resistivities, the technique may cause some circuits to lose speed when hot electrons become trapped in the oxide and shift the device thresholds. In addition, the cooled-CMOS technique will be less useful in devices with smaller geometries.

Future workstations

A topic of concern to engineers as well as to their employers—the future of the engineering workstation—will be the subject of the keynote address in **session 5**. In his speech, "Computer-based design for tomorrow's super chip," James Solomon of SDA Systems (Santa Clara, CA) will predict that by 1990, the workstation will be the accepted approach to electronic engineering. By that year, engineers will find at least $20,000 worth of computing power on their desks when they report to work, Solomon contends. Each engineer will share other equipment (worth $10,000 per engineer) over a local-area network, he predicts.

In his address, Solomon will also touch upon CAE software. He believes that these CAE tools will be so advanced in the next five years that even engineers fresh out of school will be able to tackle the ULSI (ultra-large-scale integration) chips of 1990. The CAE tools will not only make available large libraries of IC building blocks (such as PLAs, ROMs, RAMs, and data paths)—and have block compilers and macrocell place-and-route tools for assembling these building blocks—but they'll also have expert-system overlays, which will guide engineers through the complex design steps, helping them avoid known pitfalls.

Solomon will also predict a new division of labor between the IC experts at the semiconductor houses and OEM engineers. Semiconductor experts, he says, will provide the basic workstation tools and build up the libraries of IC building blocks, while OEM designers define the overall architecture of circuits on chips.

Speakers in **session 10** will offer an example of this structured-custom approach to CAE in the paper "A 32-bit digital-signal processor for motor control." The paper, a joint project by J B Costello and J T Santos of SDA Systems with some authors from National Semiconductor, will propose a universal 1-chip implementation of the electronic portion of dc-motor-position servos. The 28-pin, NMOS LM628/629 accepts position commands from a host μP and generates the trapezoidal motion profile needed to accelerate the motor to the maximum allowed speed and then decelerate it so it stops in the desired position. The LM628's internal, dedicated μP and firmware computes the motion profile and the servostability equalization in DSP fashion. To maintain the accuracy required for large and small position increments, the μP has a 16×16-bit multiplier and a 32-bit ALU.

According to the National designers, the SDA workstation approach allowed them to size the computing and memory functions to the task, keeping chip size—and cost—down. The CAE tools also allowed the designers to develop special variations of the LM628/629 quickly. For example, the designers could incorporate the commutation electronics for a brushless, Hall-effect dc motor on the chip.

A less costly implementation of CAE will be presented in the paper "Reconfigurable logic arrays" in **session 18.** This CAE implementation will allow engineers to do all design and device programming at their desks on an IBM PC. The software resides on four floppy disks; a board that plugs into one of the PC's expansion slots does the device programming. These user-alterable logic devices are becoming popular because they suit both short production runs and breadboarding, thus sparing the designer the chore of wiring TTL.

Another paper in the session, "CMOS erasable programmed logic with zero standby power," will explain how to keep chips turned off

ISSCC '86 schedule details

The 1986 International Solid State Circuits Conference will take place from February 18 to 21, 1986, at the Anaheim Hilton Towers Hotel, Anaheim, CA. Consult the **schedule** for the times and locations of the technical sessions and informal discussions. You can register for the conference sessions on Tuesday from 4 to 8 PM or on Wednesday through Friday from 8 AM to 4 PM at the hotel's second-floor promenade.

Advance registration fees (before February 7) are $90 for IEEE members, $110 for nonmembers. After February 7, those registration fees will be $100 and $120, respectively. Each registrant will receive a copy of the *Digest of Technical Papers;* additional copies cost $60 for members, $70 for nonmembers, and $20 for students who attend the conference.

ISSCC '86 AT ANAHEIM HILTON HOTEL/ANAHEIM, CA

		CALIFORNIA PAVILION A-B	CALIFORNIA PAVILION C	CALIFORNIA PAVILION D	PACIFIC BALLROOM A-B	PACIFIC BALLROOM C	PACIFIC BALLROOM D	HUNTINGTON
WEDNESDAY, FEBRUARY 19	9:00 AM 11:45 AM	—	SESSION I ANALOG TECHNIQUES	SESSION II PROCESSORS/ COPROCESSORS *	TV THEATER * TV THEATER **	SESSION III NONVOLATILE AND APPLICATION-SPECIFIC MEMORIES	—	—
	12:00 PM 1:30 PM LUNCH	—	—	—	—	—	—	—
	1:30 PM 2:05 PM	SESSION IV FORMAL OPENING */**			TV THEATER *	—	—	—
	2:10 PM 2:50 PM	SESSION V KEYNOTE ADDRESS */**			TV THEATER **	—	—	—
	3:20 PM 6:00 PM	—	SESSION VI OPTICAL LINKS	SESSION VII SEMICUSTOM ARRAYS *	—	SESSION VIII SIGNAL PROCESSING **	SESSION IX SENSOR INTERFACE	—
	6:15 PM 7:15 PM	—	—	—	—	—	—	AUTHOR INTERVIEWS
		INFORMAL DISCUSSION SESSIONS						—
	8:00 PM	WE 1 DSP ARCHITECTURE	WE 2 TESTING	WE 3 4M- TO 16M-BIT DYNAMIC RAMs	—	WE 4 HIGH-PERFORMANCE STATIC RAMs	WE 5 µPs IN 2001	—
THURSDAY, FEBRUARY 20	9:00 AM 12:15 PM	—	SESSION X SPECIAL-PURPOSE PROCESSORS AND CONTROLLERS	SESSION XI DATA ACQUISITION *	TV THEATER * TV THEATER **	SESSION XII IMAGE PROCESSING **	SESSION XIII VLSI MODELING AND PACKAGING	—
	12:15 PM 1:30 PM LUNCH	—	—	—	—	—	—	—
	1:30 PM 5:00 PM	—	SESSION XIV VOICEBAND TELECOMM ICs	SESSION XV HIGH-SPEED DIGITAL CIRCUITS AND TECHNOLOGY *	TV THEATER * TV THEATER **	SESSION XVI STATIC RAMs **	—	—
	5:15 PM 7:00 PM	—	—	—	—	—	—	AUTHOR INTERVIEWS
		INFORMAL DISCUSSION SESSIONS						—
	8:00 PM	THE 6 RISC	THE 7 ISDN	THE 8 ASIC MEMORIES	—	THE 9 POWER SUPPLIES	THE 10 LIQUID-NITROGEN CMOS	—
FRIDAY FEBRUARY 21	9:00 AM 12:15 PM	—	SESSION XVII ANALOG PROCESSORS	SESSION XVIII RECONFIGURABLE LOGIC ARRAYS *	TV THEATER * TV THEATER **	SESSION XIX DYNAMIC RAMs **	—	—
	12:15 PM 1:15 PM	—	—	—	—	—	—	AUTHOR INTERVIEWS

(ASTERISKS IN TV THEATER AREAS INDICATE SESSIONS TO BE NETWORKED FOR TV/AUDIO)

until an input transition is detected. Although the part the paper describes is fabricated in CMOS, the programmable array itself is in NMOS (UV-EPROM) technology, and it has sense amplifiers, which also consume power. The paper will examine a method of keeping these power-consuming elements turned off except when logic transitions are detected at the inputs.

The future ISDN

Future computers and workstations may well be linked to the rest of the electronic world via the integrated services digital network (ISDN). This proposed system would effect a complete end-to-end digitization of the world's telephone network, as panelists in Thursday evening's discussion "ISDN: The future for telecomm VLSI" will explain.

However, according to moderator Michael Foster of Mitel Corp (Kanata, Ontario, Canada), a few problems are delaying the implementation of the ISDN at present. First, in order to be a cost-effective replacement for the present analog channels, the ISDN will require single-chip (or few-chip) VLSI circuits. IC manufacturers, however, are hesitant to design these complex ICs until the various ISDN standard committees agree upon all the ISDN standards. At present, the North American standards committees are trying to balance sophistication and economy in the coding of the signals that go on the 2-wire U link between a telephone company's central station and a subscriber's line.

Despite the problems with ISDN standards, Foster says, progress with the network is being made. A number of telephone companies are working with various suppliers to set up ISDN trials. In addition, a number of PBX makers are already introducing ISDN concepts in their own equipment, for which they set the standards.

The potential of the ISDN market, for both semiconductor manufacturers and OEMs, will be very great, says panelist Thomas Ladshaw of Lear Siegler (Anaheim, CA). "There are over 100 million phones out there in the US alone, and if just a small percentage of those convert initially to ISDN—say, just the business users—it's still an extremely big market," Ladshaw says.

Foster and Ladshaw agree that when the problems with defining the ISDN standards are resolved, telephone companies will make steady progress in converting the existing telephone networks to ISDN. For one thing, the companies won't have to install any new copper wires: ISDN can use the existing 2-wire loops that go to all phones. And then, the telephone companies will be able to convert their networks to ISDN gradually. They can start by setting up a few ISDN racks in their central stations and connecting only those users who want ISDN services.

Further, Foster says, although the average homeowner might not need to have two 64k-bps ISDN voice and data channels coming into his or her home, third parties that could benefit from such channels might underwrite some of the cost. Utility companies, for instance, could save money by reading meters over ISDN's D control channel. The D channel could also provide a homeowner with communication links to firefighters and police.

These informal discussion sessions—along with the technical sessions on such topics as analog techniques, nonvolatile and application-specific memories, semicustom arrays, DSP architecture, data acquisition, image processing, high-speed digital circuits, high-performance static RAMs, and dynamic RAMs—will inform attendees of ISSCC '86 about recent innovations in technological research and give them a foretaste of future developments. **EDN**

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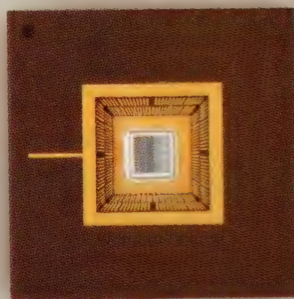

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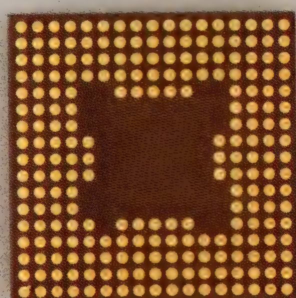

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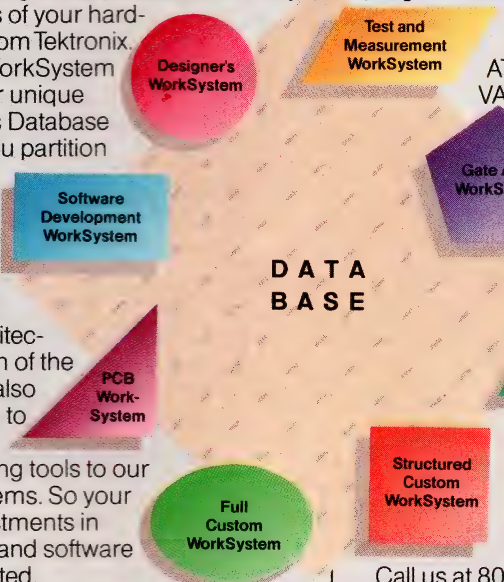

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Bering Series 8000-EPs and TopSecret Removable Hard Disk Subsystems are HP-IB compatible and designed for any HP computer using CS/80 and SS/80 command sets.

from two new mass storage solutions from Bering Industries. The Series 8000-EP and TopSecret Removable Hard Disk Subsystems. Designed for HP computers using CS/80 and SS/80 command sets, like HP1000, HP3000, and HP9000 Series 200/300/500 systems.

Enhanced Performance 8000-EP

Bering's Series 8000-EP enhanced performance hard disk subsystems offer an alternative HP mass storage solution. From 65MB to 190MB, the EPs are worth a close look.

Cost Savings. At $60 per MB, EPs are price/performance leaders. Savings can be up to 45% the cost of a comparable HP drive. And Bering's standard one-year warranty applies to all EP models.

Capability. Designed for HP users' critical performance needs in real-time and multi-user environments, the EPs are the best choice. An advanced disk controller and fast head seek mechanism match average transfer rates of HP7912/7914 drives.

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Data Security. Securing classified data is easy with 5.25″ TopSecret removable hard disks. Sensitive information can be locked away in a safe, 10MB at a time. Personal data storage and selective file back-up is convenient and fast.

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Bering has set the pace for innovative mass storage solutions in the HP world since 1981. Bering is an official HP Independent Hardware Vendor with authorized service and support by DATAGATE in the USA, and by DATATECH in Canada. For complete specifications on the EPs, the TopSecret, and 100 other disk configurations, call or write us today!

Note: HP, CS/80, SS/80, and HP-IB are tradenames of Hewlett-Packard Company.

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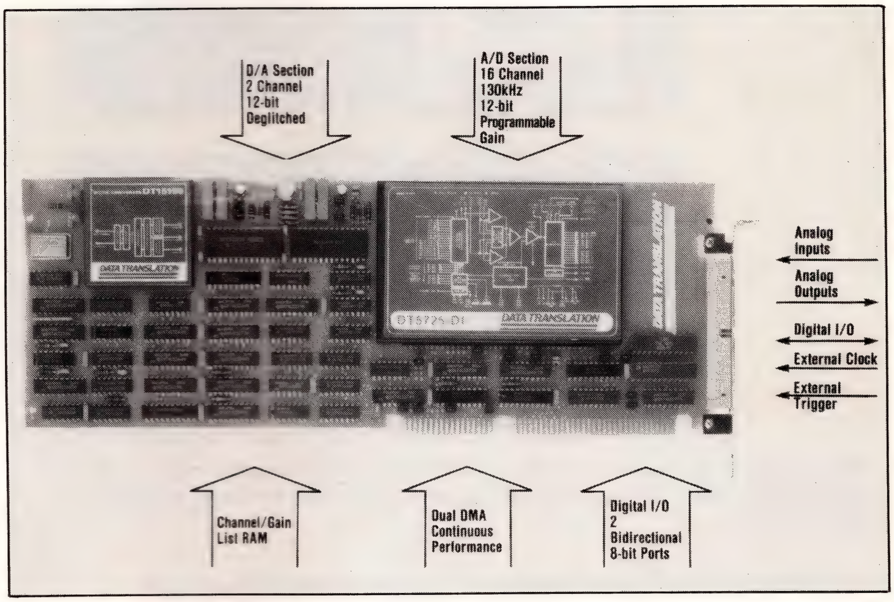
Telex: 325606
415/651-3300

PC/AT-compatible data-acquisition board has 12-bit analog I/O, 130-kHz throughput

The DT2821 12-bit data-acquisition board, which plugs into a card slot in the IBM PC/AT and clones, performs conversions at rates as high as 130 kHz. This conversion rate represents a quantum leap over that of earlier cards, which provide 50-kHz max throughput. Model DT2821-F-16SE accepts 16 single-ended inputs, and the DT2821-F-8DI has eight differential-input channels.

The key to the speed of the system's analog-to-digital conversion is the manufacturer's DT5725 analog-input module (see "Modular analog-input and -output units provide high speed and resolution," EDN, August 8, 1985, pg 97). This 150-kHz module contains the multiplexer, instrumentation amplifier, track/hold amplifier, A/D converter, and control logic needed to perform the DT2821's data-acquisition function.



Boasting the highest speed in the industry, *the DT2821 data-acquisition board brings analog-I/O capabilities to the IBM PC/AT and clones. Its 130-kHz throughput rate stems from the manufacturer's high-speed analog-input module. The unit accommodates 16 channels of data in the single-ended version and eight channels in the differential-input version. You can use the system in programmed-I/O or DMA mode.*

You use a 2-bit code to program the instrumentation amplifier's gain to 1, 2, 4, or 8. Input range is jumper selectable to ±10V or 0 to 10V; division by the selected gain value yields the effective input range. A 4-bit word selects the channel to convert.

Unit has RAM channel/gain list

A convenient feature in the DT2821 is a RAM channel/gain list. This block is a 16-location RAM that you can use to specify the sequence of channels and the gain at which the system will sample each channel. When an A/D-conversion scan begins, the board sequences through the RAM, sampling each channel entry at the specified gain. The RAM allows you to predefine virtually any desired sampling sequence: sequential sampling (0 to n or n to m channels, for example), random channel sampling (eg, channels 0, 3, 2, 5), or successive samples on a single channel at the same or different gain.

In addition to the A/D converter, the DT2821 contains two independent 12-bit D/A converters. You can control the D/A section in either programmed-I/O or DMA mode. The A/D and D/A converters have sufficient differential linearity to guarantee no missing codes and monotonicity (respectively) over 0 to 70°C. The D/A converters are low-glitch types: Glitch area is typically 3 mV·µsec. You use jumpers to select unipolar output ranges of 0 to 5V or 0 to 10V; bipolar ranges are ±2.5, ±5, or ±10V.

Card has five interrupt levels

The data-acquisition card accommodates interrupts to the PC/AT's processor upon the completion of significant events. The board's interrupt source, selected under program control, includes A/D done (programmed I/O transfers); A/D DMA done (DMA transfers); A/D scan done; A/D error; D/A ready (programmed I/O transfers); D/A DMA done; and D/A error. The DT2821 can interrupt the processor on any of five levels (from highest to lowest): 10, 15, 3, 5, or 7. You use a jumper to select the interrupt level.

Continuous-performance DMA operation allows the DT2821 to perform gap-free DMA transfers of large amounts of data. Data is transferred through a pair of buffers, each associated with a separate DMA channel. The transfers require both buffers: Upon reaching the end of the first buffer, the system shifts automatically to the second buffer without pausing or missing any samples.

You can use the onboard pacer clock to initiate A/D, D/A, or concurrent A/D and D/A conversions.

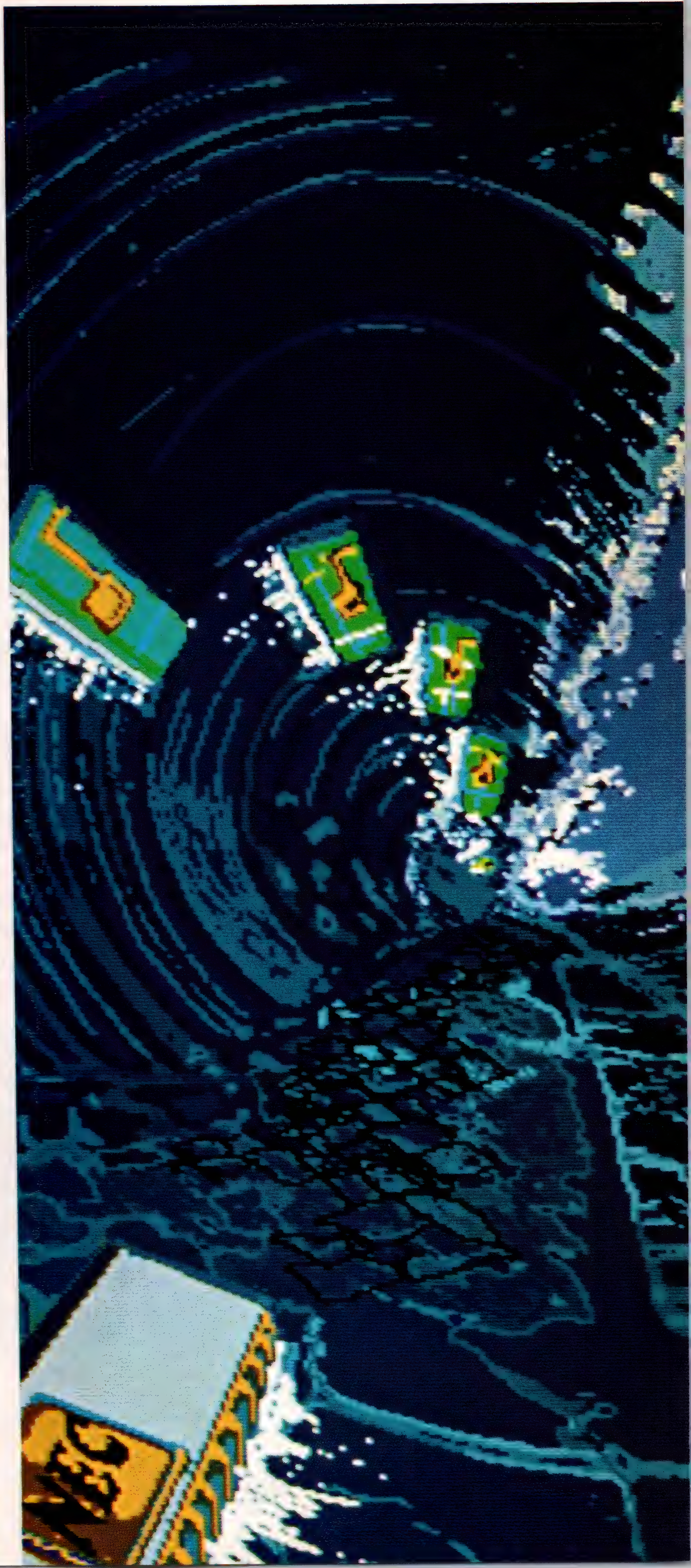
The clock comprises three elements: a 6-MHz pulse generator, a clock prescaler that serves as a programmable divider, and a counter divisor. You can set the prescaler in powers of 2 from 0 to 31. The counter divisor is an 8-bit programmable counter that divides the prescaler's output by a number from 1 to 256.

ATLAB, a real-time software package from the DT2821's maker, accommodates Call commands from Fortran, C, and Pascal. The software provides library routines for control of all the system's analog- and digital-I/O functions. An error-processing system checks for argument errors and generates error reports. The system reports—and refuses to obey—attempts to operate the board in illegal modes of operation.

Several screw-terminal and signal-conditioning panels are available from the manufacturer. The 130-kHz DT2821 costs $1595, and ATLAB is priced at $449. A 50-kHz version of the DT2821 has all the features of the higher-speed units and costs $1195.—***Bill Travis***

Data Translation Inc, 100 Locke Dr, Marlboro, MA 01752. Phone (617) 481-3700.

Circle No 729



Wireless modem and portable computer provide secure, encrypted network

Using packet radio-transmission technology to eliminate the cables commonly associated with local-area networks (LANs), the Esteem Model 85 wireless modem and Quest wireless portable computer team up to create a mobile, encrypted LAN with a communication range as great as 50 miles.

The Model 85 modem offers you 50 channels and a 1k-byte data spooler, yet consumes only 1W. The device's effective baud rate is 2817 bps—a slow rate compared to those of cable-based LANs like Ethernet, which boast data rates of 9600 bps and greater. The 2817-bps rate is, however, much faster than the ubiquitous 300- and 1200-bps modems that operate via telephone lines. Furthermore, this radio modem eliminates the considerable expense of laying cables or wires.

The Z80-based modem uses packet radio techniques to transmit rapid bursts of tightly grouped data. Prior to transmission, the modem compresses and encodes the data, via the High Level Data Link (HDLC) format, into compact frequency-modulated packets of 504 bytes each. The modem then runs the HDLC format through a Manchester coder and transmits the data. The receiving radio modem uses 16-bit error-correction algorithms to screen the incoming packets for bad data. If it detects an error, the receiving unit sends a retransmission signal to the sending unit, and the sequence begins again.

Each modem has a unique address, and each provides network management for as many as 254 terminals. DIP switches on the Model 85's back panel allow you to set the baud rate and radio frequency. You can adjust the baud rate to allow the modem to communicate with other devices via an RS-232C port at 19k bps in full-duplex mode. You can also select a radio communication frequency between 72.04 and 72.96 MHz at 40-kHz intervals.

You can develop a LAN without telephone connections *or costly cabling by using the wireless Model 85 modem. You can rearrange the communications network just by moving your RS-232C-compatible equipment to a new location.*

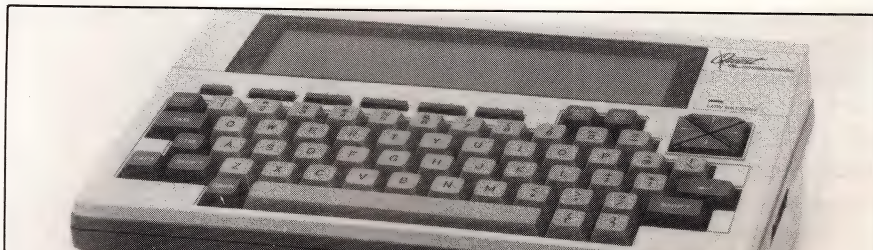
The Model 85 offers an impressive level of data security. Each modem transmits on one of 50 frequencies and has one of 254 addresses, so each unit offers 12,700 possible frequency-address combinations. A person couldn't eavesdrop on your data transmission simply by buying a radio modem and determining your particular frequency and address—the individual would still have to synchronize his system with the random bursts of data from your packet radio transmission. For even greater data security, you can order an encryption board that meets the National Bureau of Standards' information-processing data-encryption standard No 46.

The Quest radio computer is a logical companion to the Model 85 modem. The 7-lb computer has a 1-in. base that contains a battery pack and radio modem. It comes with 16k bytes of RAM that's expandable to 96k bytes, an 8-line×40-character LCD, a full-size keyboard, ROM-based text editing, Basic, a scheduler, and telecommunications software.

Together, the modem and computer form a network that's completely free of the limitations of power cords and communication cables. Further, the radio-based network lets you mix hardware from a variety of manufacturers without worrying about software incompatibility. Model 85, $1200; Quest, $2295.—***J D Mosley***

Electronic Systems Technology, 1031 Kellogg St, Kennewick, WA 99336. Phone (509) 735-9092. TLX 152514.

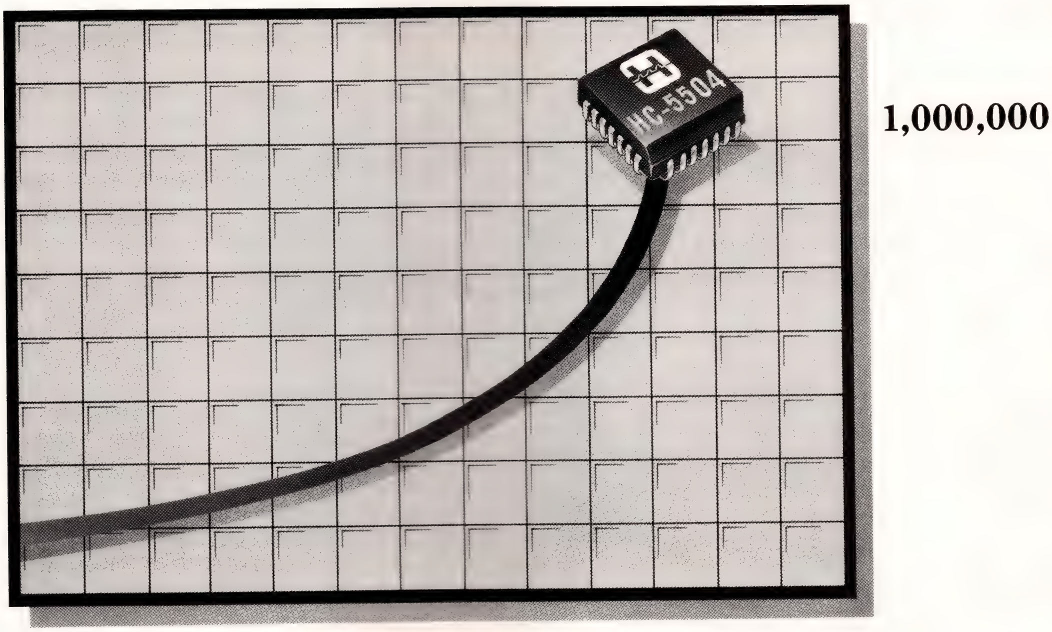
Circle No 727



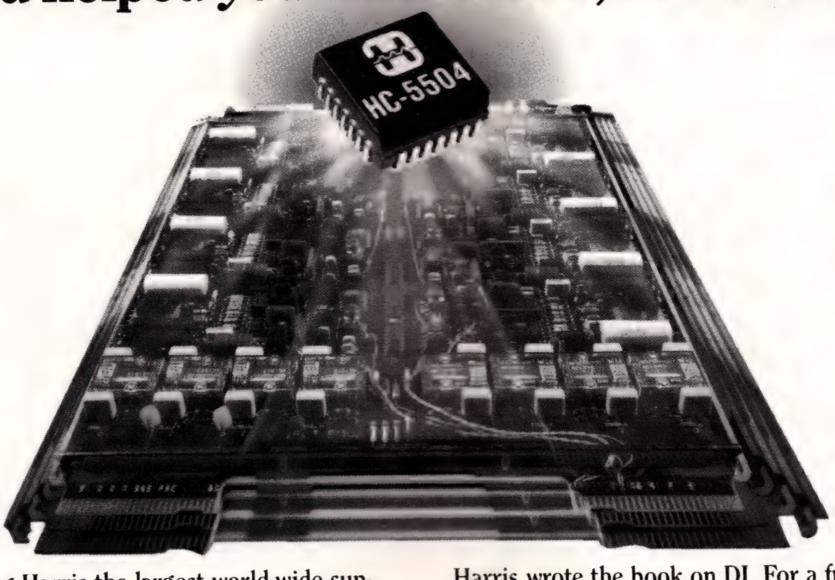
Suitable for mobile data communications, *the Quest portable computer needs no power outlets, telephone wires, or network cabling to establish a computer link with other equipment.*

Thank You, Telecom Designers

We just delivered our millionth SLIC...



and helped you shrink 100,000 boards!



Thank you for making Harris the largest world-wide supplier of solid-state Subscriber Line Interface Circuits. You've discovered our Dielectric Isolation process is the perfect solution for high-voltage line interface problems. You've seen how DI offers you the performance, reliability, and space savings you need, all at lower cost and proven out by volume production. You've continued to look to Harris for the "solid-state of the art" in telecom designs — because while others talk SLICs, Harris delivers.

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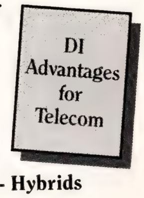


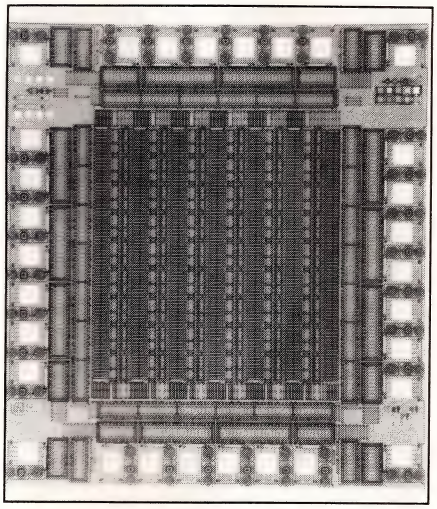
Harris Semiconductor: Analog - Bipolar Digital CMOS Digital - Gallium Arsenide - Semicustom - Custom - Hybrids

HARRIS

For your information, our name is Harris.

18V linear/digital CMOS arrays implement automotive- and industrial-control circuits

Series MH silicon-gate CMOS arrays operate with supply-voltage levels as high as 18V, suiting them for automotive- and industrial-control applications. The center of each array contains transistors organized to implement digital gates. Around the periphery are larger transistors suitable for implementing output drivers and linear circuits. In addition, digital cells by the output pads can implement I/O circuits or logic gates, increasing the capability of the array.



Analog components surround digital gates *on MH Series arrays. Built to operate with 18V supply levels, the arrays are suitable for automotive- and industrial-control applications.*

I/O cells implement logic

The series consists of eight arrays that vary in complexity from 70 to 1600 equivalent 2-input gates and 18 to 84 I/O pads (**Table 1**). An I/O cell at each pad contains diodes that protect against voltage extremes and an npn transistor that can supply 10 mA. In addition, the I/O cells contain digital circuitry that can implement input, output, and bidirectional buffers. Peripheral circuitry not used for I/O can implement logic functions; for example, you can build four NAND gates or a D-type flip-flop in an I/O cell if the cell is serving as an input buffer. The peripheral circuitry makes the logic complexity of the arrays higher than their listed number of equivalent gates.

You can create analog circuits from the I/O circuitry as well. Although the vendor includes no analog cells in its function library, you can build such linear circuits as current mirrors, op amps, and D/A converters from the transistors on the periphery of the arrays. The vendor plans to develop and offer analog cells this year.

The vendor currently supplies a library of digital macro functions (cells) for Mentor and FutureNet workstations for logic and circuit design. Alternatively, the company can supply you with its CAE software, or it can perform the design for you. The library contains 50 functions that the company modeled after standard Series 4000 CMOS parts. Once you've settled on your logic design, the company performs all layout tasks and submits final performance estimates for your approval. Turnaround time for prototypes, including layout, is six to 16 weeks, depending on design complexity and on how much of the design the company performs.

TABLE 1—MH SERIES CMOS ARRAYS

ARRAY	I/O PADS	EQUIVALENT GATES	SMALLEST PACKAGE (PINS)
MHA	18	70	8
MHB	24	140	8
MHC	30	200	14
MHD	40	330	14
MHE	48	500	14
MHF	56	660	22
MHG	68	1000	22
MHH	84	1600	22

Many package types available

The vendor packages the arrays in DIPs, small-outline packages, surface-mount carriers, chip carriers, and pin-grid arrays. Plastic and ceramic versions are available for many packages. The DIPs have pin counts as high as 48, and chip carriers and pin-grid arrays can supply as many as 84 pins. The manufacturer can perform all processing, packaging, and screening in accordance with MIL-STD-883C requirements.

Nonrecurring engineering (NRE) charges start at $5000, and unit prices start at $1 (for 10,000 MHA arrays in 14-pin plastic DIPs).

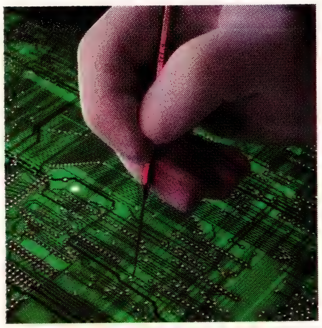
—David Smith

Ferranti Interdesign Inc, 1500 Green Hills Rd, Scotts Valley, CA 95066. Phone (408) 438-2900.

Circle No 726

No "boomerang effect" at Trend Circuits. Less than 1% of our prototype boards ever come back.

Fast turnarounds in prototype circuit boards are great — but not when the boards circle back again and again because of poor quality.



That "boomerang effect" costs precious time in proving your concepts and can end your chances to meet critical market windows.

We deliver speed *and* quality.

Speedy turnarounds don't count for much if prototypes don't work. At Trend Circuits, we're specialists in rapid production of prototype boards that work first time out. That's because we're people who understand your language, your objectives and your pressures.

Further, fully one-third of our people are involved in inspection. We begin with incoming artwork, where we can quickly identify common design errors. And we continue with double- and triple-checking right through to completion. As a result, less than a scant 1% ever come back. And that's good for both of us.

Now for speed. On a regular basis, we deliver *double-sided boards within 24 hours, and multi-layer boards within five days.* In fact, we're completing no less than 82% of all our work within five days.

Check our references.

You can verify our facts easily enough by talking to our customers. Simply phone and we'll put you in touch with people who've decided they won't accept compromise in quickly moving from design to finished prototype. They'll tell you why we're their logical choice for "no-boomerang" boards. And why we should be yours.

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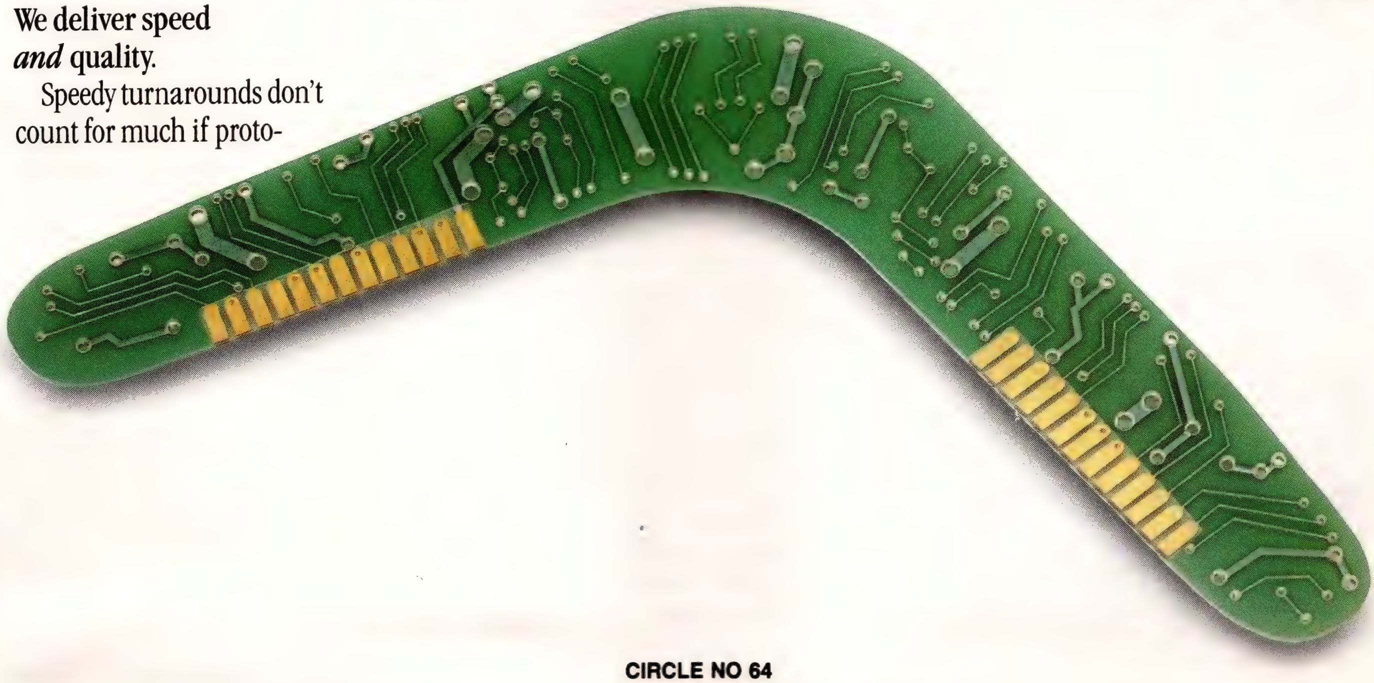
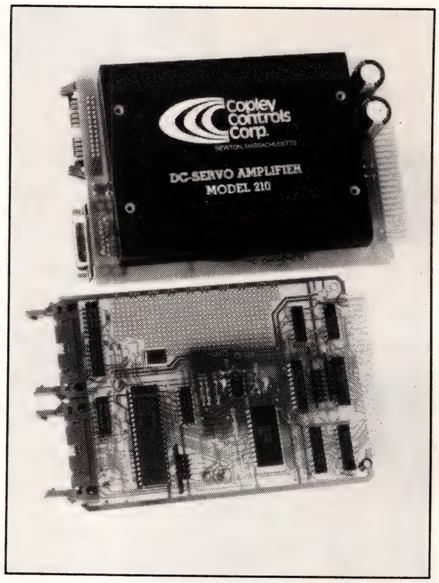


CIRCLE NO 64

Motion-control subsystem is STD Bus compatible

Model 450/451/452 2-card servo-I/O subsystem includes a general-purpose motion controller and a pulse-width-modulated (PWM) servo amplifier. You can use the system as a complete single-axis drive controller for dc motors. The controller is compatible with the STD Bus; it accepts commands from either the bus, an RS-232C serial input, or local switches.

The 450 Series controller is a microprocessor-based system that can control motor position, velocity, and torque. The system generates a trapezoidal velocity profile that has programmable acceleration and slew rates. The system, which needs no analog feedback, owes its stability to digital filtering. You can vary the filter's coefficients to suit particular robotics and automation applications.



***High-power motor control in a small package** and STD Bus compatibility are the hallmarks of Series 450 motion-control subsystems. The 2-card set can control loads demanding power as high as 500W, yet the output amplifier dissipates only 12W, because the switching elements are power MOSFETs.*

Residing on a second card, the PWM output amplifier is available in three ratings. Model 450 contains an amplifier that can drive motor loads requiring 5A peak and 2A continuous current at voltages from 15 to 45V. Models 451 and 452 both accommodate voltages of 15 to 75V; the 451 provides currents of 10A peak, 4A continuous; the 452 controls 20A peak, 7A continuous current.

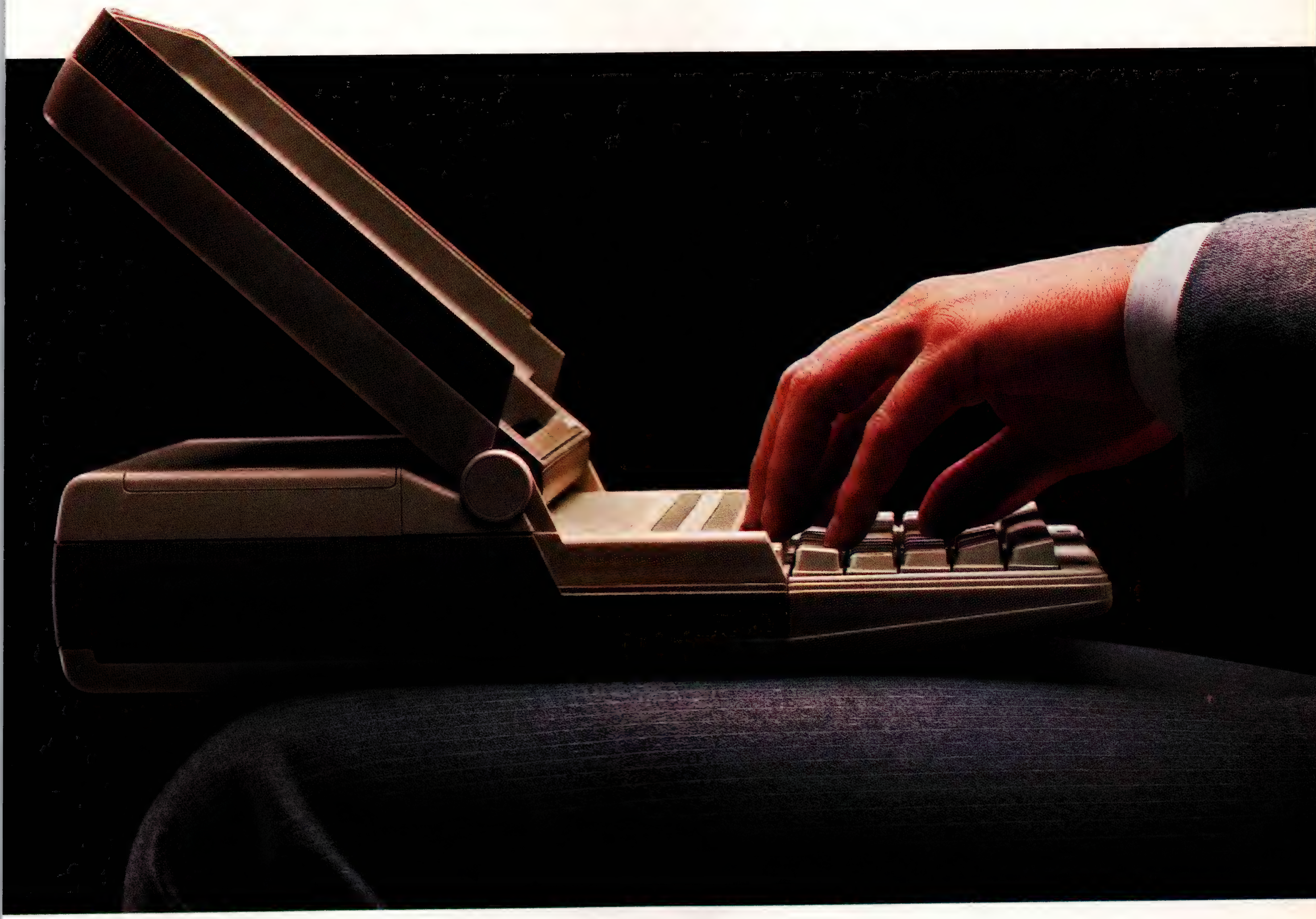
To avoid generating acoustical switching noise, the PWM amplifiers use a 22-kHz switching frequency. This high switching frequency also allows you to dispense with a series choke in applications using low-inductance motors. A power-MOSFET bridge in the amplifier's output circuit provides high-efficiency switching—for example, Model 452 dissipates only 12W while providing 500W output power. An internal dc/dc converter generates all bias voltages needed on the amplifier card.

All Series 450 controllers operate over 0 to 70°C without derating. Required power supplies are 5V and ±12V for the controller card and 15 to 45V (Model 450) or 15 to 75V (Models 451 and 452) for the PWM servo-amplifier card. Prices for the 450, 451, and 452 2-card systems are $995, $1085, and $1175, respectively.—***Bill Travis***

Copley Controls Corp, 375 Elliot St, Newton, MA 02164. Phone (617) 965-2410.

Circle No 728

THE FIRST SINGLE-CHIP MODEM SOLUTION JUST FELL INTO YOUR LAP.



For truly portable, battery-powered data processing applications, you really need a full-featured single-chip modem. Especially if you're designing laptop computers.

And the fact is, you don't have many choices.

So go with the first choice: Fairchild's new μA212A.

It's perfect for laptop PCs because it's the first single-chip, Bell 212A-compatible modem IC with 1200/300 bps full duplex transmission. And power consumption? The μA212A, made with our high-performance, double-poly silicon-gate CMOS process, features a typical power consumption of only 45 mW. And it performs all the signal processing functions singularly, compared to the competition's solutions requiring up to five chips.

Now designing with modems is easier and faster than ever before. Particularly in applications such as desktop PCs and workstations, voice/data terminals, hand-held terminals, remote diagnostics, instrumentation, and stand-alone modems. And we back the μA212A with Fairchild's comprehensive design and customer support.

For more details on the new μA212A, simply contact The Fairchild Customer Information Center at 1-800-554-4443.

The Fairchild single-chip modem. It'll put all your modem designs in the lap of luxury.

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LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	5	19	67	9	0	0	7.2	9.7
Pot-Core	0	7	73	20	0	0	9.2	8.5
Laminate (power)	6	18	47	29	0	0	8.8	8.8
CONNECTORS								
Military panel	0	33	67	0	0	0	6.0	10.6
Flat/Cable	6	55	39	0	0	0	4.2	5.4
Multipin circular	11	33	28	28	0	0	7.3	8.8
PC	0	55	36	9	0	0	5.4	4.3
RF/Coaxial	21	29	29	14	7	0	7.0	7.1
Socket	26	37	37	0	0	0	3.6	4.2
Terminal blocks	16	47	37	0	0	0	3.8	4.3
Edge card	17	39	44	0	0	0	4.3	6.2
Subminiature	15	21	43	14	7	0	8.0	6.7
Rack & panel	0	63	37	0	0	0	4.2	6.0
Power	0	78	22	0	0	0	3.3	6.6
PRINTED CIRCUIT BOARDS								
Single-sided	0	64	36	0	0	0	4.1	3.7
Double-sided	0	50	43	7	0	0	5.5	5.3
Multilayer	6	0	69	25	0	0	9.5	7.2
Prototype	4	80	8	4	4	0	3.9	2.7
RESISTORS								
Carbon film	36	36	19	9	0	0	3.6	2.7
Carbon composition	31	31	23	15	0	0	4.9	3.8
Metal film	10	38	31	21	0	0	6.5	3.9
Metal oxide	8	50	42	0	0	0	4.3	3.2
Wirewound	9	27	35	9	0	0	6.3	8.1
Potentiometers	14	32	41	9	4	0	6.5	3.9
Networks	17	35	35	9	0	4	6.2	5.1
FUSES	32	54	14	0	0	0	2.1	2.6
SWITCHES								
Pushbutton	27	27	41	5	0	0	4.5	3.5
Rotary	11	22	56	11	0	0	6.6	4.2
Rocker	9	36	36	19	0	0	6.5	5.3
Thumbwheel	10	30	30	30	0	0	7.8	7.1
Snap action	25	25	33	17	0	0	5.8	4.9
Momentary	23	39	23	15	0	0	5.0	6.1
Dual-in-line	15	50	21	14	0	0	5.0	5.2
WIRE AND CABLE								
Coaxial	22	50	21	7	0	0	3.8	2.5
Flat ribbon	25	60	15	0	0	0	2.4	3.1
Multiconductor	18	47	23	0	0	0	4.7	4.1
Hookup	52	33	15	0	0	0	1.8	1.3
Wire wrap	15	70	15	0	0	0	2.6	1.7
Power cords	16	58	21	5	0	0	3.6	3.8
Other	11	44	33	0	12	0	6.4	6.6
POWER SUPPLIES								
Switching	0	25	58	8	9	0	8.6	8.4
Linear	0	25	75	13	0	0	6.5	6.1
CIRCUIT BREAKERS	0	54	31	15	0	0	6.0	5.8
HEAT SINKS	18	55	18	9	0	0	4.0	3.9

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
General purpose	26	26	32	16	0	0	5.5	4.8
PC board	0	50	25	25	0	0	7.0	6.3
Dry reed	0	37	63	0	0	0	5.7	4.6
Mercury	0	25	75	0	0	0	6.5	6.3
Solid state	0	40	33	27	0	0	7.7	6.4
DISCRETE SEMICONDUCTORS								
Diode	30	27	34	9	0	9	4.6	5.0
Zener	21	18	54	7	0	0	5.7	4.0
Thyristor	6	35	47	12	0	0	6.3	4.2
Small signal transistor	20	20	48	12	0	0	6.3	4.2
FET, MOS	14	36	36	7	7	0	6.7	5.6
Power, bipolar	29	14	29	21	7	0	7.8	5.9
INTEGRATED CIRCUITS, DIGITAL								
CMOS	18	21	32	21	4	4	8.4	5.1
TTL	32	12	24	32	0	0	7.2	5.8
LS	25	20	30	25	0	0	6.8	6.0
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	33	50	17	0	0	7.3	6.0
OP amplifier	25	25	30	15	5	0	6.6	5.8
Voltage regulator	23	23	45	5	4	0	6.0	5.0
MEMORY CIRCUITS								
RAM 16k	39	22	22	17	0	0	4.9	5.1
RAM 64k	38	31	15	16	0	0	4.3	4.4
RAM 256k	18	45	18	19	0	0	5.3	5.7
ROM/PROM	18	18	45	19	0	0	6.9	7.2
EPROM	23	31	23	23	0	0	6.2	6.0
EEPROM	34	0	33	33	0	0	8.0	5.7
DISPLAYS								
Panel meters	27	27	27	19	0	0	5.6	5.0
Fluorescent	0	50	25	25	0	0	7.0	6.1
Incandescent	14	57	29	0	0	0	3.4	5.3
LED	30	25	40	5	0	0	4.5	5.3
Liquid crystal	18	19	64	9	0	0	6.7	8.2
MICROPROCESSOR ICs								
8-bit	23	6	53	18	0	0	7.2	6.9
16-bit	21	14	36	22	7	0	8.4	7.9
FUNCTION PACKAGES								
Amplifier	44	0	45	11	0	0	5.3	6.8
Converter, analog to digital	8	42	33	17	0	0	6.2	6.7
Converter, digital to analog	8	42	33	17	0	0	6.2	6.7
LINE FILTERS	25	0	50	25	0	0	8.0	5.4
CAPACITORS								
Ceramic	21	29	46	4	0	0	4.9	5.2
Ceramic monolithic	28	24	43	5	0	0	4.7	5.2
Ceramic disc	19	28	48	0	5	0	5.6	3.5
Film	23	27	36	9	0	5	6.3	4.8
Electrolytic	15	26	48	11	0	0	6.1	5.5
Tantalum	12	12	63	13	0	0	7.3	5.3
INDUCTORS	22	17	50	5	6	0	6.7	4.0

Source: *Purchasing* magazine's electronics business survey

ABBOTT DELIVERS ITS FIRST PAIR OF TRIPLES.

ABBOTT'S NEW TRIPLE OUTPUT, 200 kHz 100-WATT SWITCHING POWER SUPPLY SERIES.

In response to the critical need for low profile, triple output, high switching frequency power supplies for use in airborne, shipboard or ground support installations, Abbott has created two new 100-watt switchers that live up to our reputation—"When reliability is imperative."

Triple output, low ripple and noise specs combined with hermetic seal construction make both WM100T and MB100T perfect for powering digital integrated circuitry, logic circuits, data processing and retrieval, sonar, radar, communications and electronic countermeasures equipment.

Designed for the military environment, model WM100T, optimized for an airborne environment, accepts a 400 Hz input. For naval applications model MB100T accepts a 60 Hz input, while both deliver 100 watts in a high-density package of 1.875" x 4" x 7.5".

Standard features include short circuit protection and remote error sensing. Options which add extra versatility include 3-phase/wye configuration, wider input voltage range, TTL turn-on/turn-off and military connector.

And that's just the beginning. Soon Abbott will offer several additional power supply families which range from 60 to 500 watts, with single, triple and quadruple outputs to choose from. Call or write for complete specs and our new Abbott Military Power Supply Catalog today. Abbott Transistor® Laboratories, Inc., Power Supply Division, 5200 West Jefferson Blvd., Los Angeles, CA 90016 (213) 936-8185. Eastern Office: (201) 461-4411. Southwest Office: (214) 437-0697.

	WM100T	***MB100T***
Input frequency	*320-480 Hz*	*47-65 Hz*
Input voltage	*115V ac ± 10%*	
Outputs	*(5 V, ± 12 V; or ± 15 V)*	
Switching frequency	*200 kHz*	
Efficiency	*65% minimum*	
Ripple/noise	*100 mV peak-to-peak max*	
Line regulation	*10 mV (103.5-126.5 V ac)*	
Load regulation	*10 mV main (.5% aux outputs)*	
EMI	*meets MIL-STD-461B*	
Environment	*MIL-STD-810C, MIL-S-901C*	
Input protection	*MIL-STD-704*	*MIL-STD-1399*
Operating temperature range	*-55°C to 100°C*	*-20°C to 71°C*
Storage temperature range	*-65°C to 125°C*	*-55°C to 85°C*
MTBF (ground benign)*	*99,408 hours*	*97,935 hours*
MTBF (ER Option)*	*375,248 hours*	*220,434 hours*
MTBF (Naval sheltered)*		
Standard	————	*17,632 hours*
ER option	————	*34,307 hours*
MTBF (Air inhabited)*		
Standard	*14,985 hours*	————
ER option	*27,012 hours*	————

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CIRCLE NO 67

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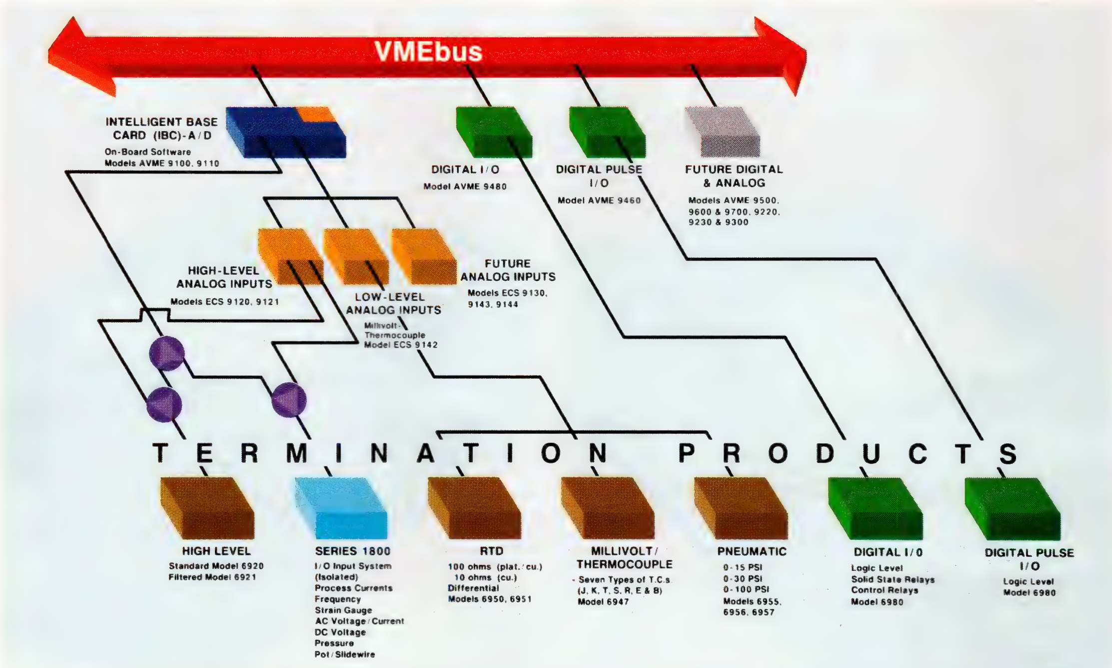
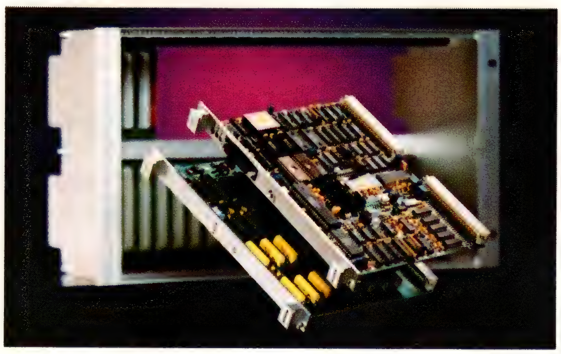


VME-Industrial I/O signal interfacing is now a simple matter of "putting it on the bus." Thanks to Acromag's analog and digital cards and termination products for interfacing real world I/O signals.

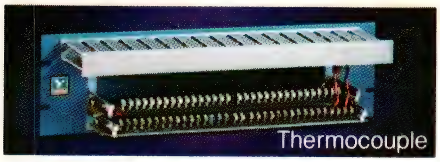


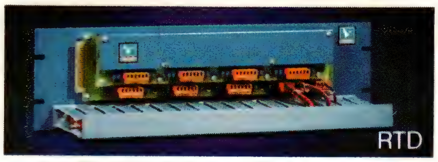
Field inputs such as thermocouple, RTD, voltage, frequency, strain gauge, pneumatic and many others are directly interfaced via screw type termination products and I/O cards to the VMEbus—as easy as IBC.

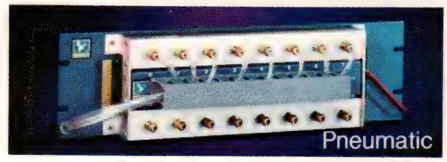
The Analog Intelligent Base Card (IBC) simplifies the problem by forming an intelligent base for the analog subsystem collecting and conditioning up to 256 analog signals and storing all in dual port RAM memory. The IBC and analog I/O cards provide for 14-bit A/D conversion, amplification, isolation, scaling, linearization and limit checking. The IBC card also has a local serial port for calibration, diagnostics and configuration.

And digital I/O? Of course... provided for by a 64 channel 30 volt bi-directional I/O card with or without relay field interfaces using a variety of screw type termination panels.

Acromag's VME cards and termination products provide the broadest industrial I/O capability available. All to make solutions to your industrial I/O needs as easy as IBC.







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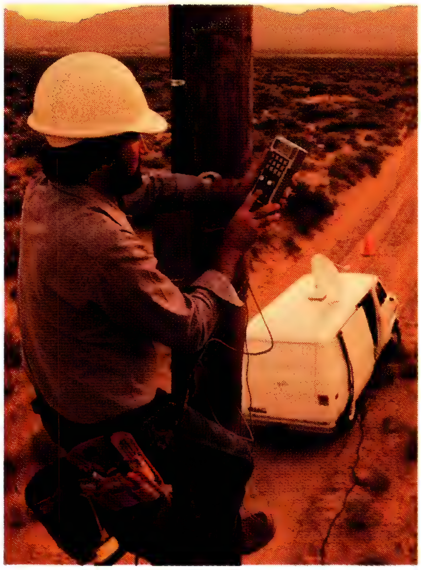
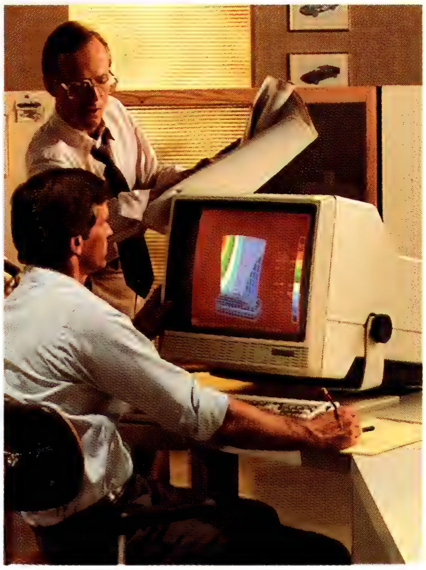
To find out more about Acromag's VME Industrial I/O capability and commitment write for Bulletin 20-000.0. Or for immediate help call our telemarketing department at 1-800-ACROMAG or (313) 624-1541.

New superfast signal processor from Texas Instruments keeps transactions strictly private...

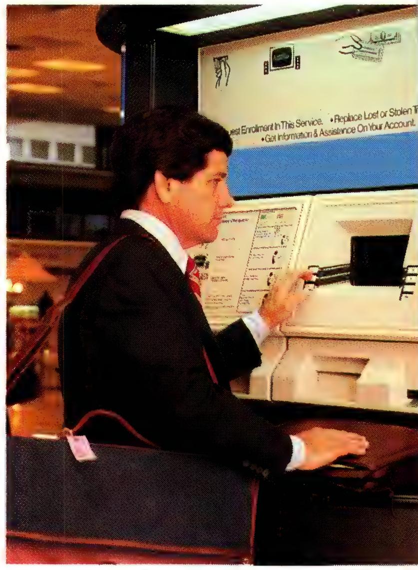
strengthens signals, enhances squelches echoes, and gets you Meet TI's new TMS32020



Echo cancellation can be greatly improved by using new TMS32020 processor, allowing telephone messages to come through loud and clear from anywhere.



Graphics systems could be economically implemented with TI's TMS32020 supplying throughput capability required for realtime rotation, scaling, and translation.



High-speed modems (4.8K bps to 19.2K bps) can be built with fewer chips and in shorter development time using TI's new TMS32020 processor.

It can handle all your digital signal processing (DSP) better than ever before. And as you will read, TI's new, single-chip TMS32020 can also be an efficient, economical processor for many high-speed, numeric-intensive applications.

And because it is available now, fully supported, the TMS32020 can speed your system development.

Up to three times faster throughput

TI's new TMS32020 processor delivers two to three times the throughput of the industry standard, TI's own TMS32010.

Behind this dramatic increase are (1) an expanded instruction set with repeat feature, (2) an expanded memory capability both on chip and off, and (3) much faster I/O.

Top secrets stay top secret when secure-telephony systems (on cover) are designed using TI's new TMS32020 signal processor. Its vastly improved throughput allows it to perform all critical subroutines so rapidly that deciphering the code is made virtually impossible.

Like the TMS32010, the TMS32020 utilizes a modified Harvard architecture emphasizing overall system throughput, communication, and flexibility in processor configuration.

Increased capability and flexibility

Having greater throughput, TI's TMS32020 makes fast work of filtering, correlation, windowing, transforms, wave-form generation, and all your other DSP tasks. 544 words of on-chip RAM, 32-bit arithmetic, single-cycle multiply/accumulate instructions, and an independent auxiliary register arithmetic unit further equip the TMS32020 for realtime DSP systems.

However, the capabilities of the TMS32020 should challenge your imagination. Its 64K word program *and* 64K data-memory spaces, timer, serial port, multiple-interrupt structure, provision for external wait states, and multiprocessor interface capability make the TMS32020 a natural choice for wide use.

And the TMS32020 is economical. Through VLSI implementation, the TMS32020 incorporates all these features into a single, 68-pin grid-array package.

Full support shortens development time

A wide range of development hardware and software tools is available to shorten your design cycle. Included are full-speed emulators, software simulators and assemblers/linkers, and application reports, plus other documentation (*see box*).

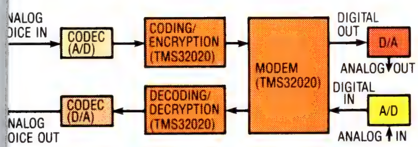
Three-day DSP workshops are conducted periodically at TI's Regional Technology Centers, and TI application engineers are also ready to provide help. Extensive third-party support is available.

A TMS32020 applications handbook and additional documentation are only 11 quick keystrokes away, 1-800-232-3200, ext. 3502, or use the coupon on page 4.

Where economy is a prime design consideration and system requirements are less demanding, use TI's industry-standard TMS32010 DSP. An extended temperature range military version is also available.

graphics, to market faster. digital signal processor chip.

TMS32020 provides all secure-telephony features



Because it can perform several functions by simply executing a variety of subroutines, TI's TMS32020 processor is a prime candidate for secure-telephony applications.

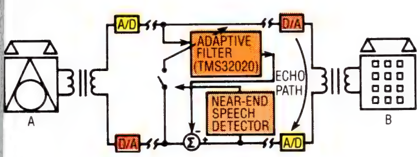
For example, multiple TMS32020s can compress the voice, encrypt the digital signals, and act as a modem.

The fast cycle time of the TMS32020 is not only essential to the encryption/decryption routine but can also allow the routine to be constantly varied so that cracking the code would be difficult.

The large program memory, serial port, and single-cycle multiply/accumulate facilitate the coding, decoding, and modem routines.

Thus, the TMS32020 is an effective alternative to the costly fully custom circuits you would have to use to gain equivalent processing power.

TMS32020 cancels echoes more accurately

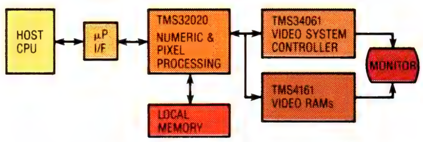


For more effective echo cancellation, the 544-word on-chip data memory of TI's TMS32020 enables it to provide larger, more accurate adaptive filters. Because of this memory and the single-cycle multiply/accumulate/data move, the TMS32020 can execute and update a 128-tap adaptive filter needed by the echo-cancellation-model routine. And the extraordinary speed of the TMS32020 allows the adaption routine to execute in real time.

The TMS32020 completes a multiply/accumulate/data move in a single cycle. Its "repeat instruction" allows the next instruction to be repeated "N" times, which saves program memory space and effectively pipelines the instruction.

In addition, the 544 words of on-chip data RAM allow quick updates of taps for faster adaptation, and the serial I/O port allows direct interface to a codec with little or no "glue" logic.

TMS32020 excels at fast matrix manipulations



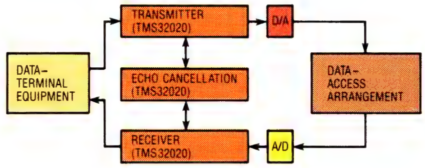
In graphics applications, TI's TMS32020 processor can be used for both numeric and pixel processing. Its 200-ns multiply/accumulate allows the TMS32020 to execute realtime graphics scaling, rotation, and translation. All depend upon memory-intensive matrix manipulations that require rapid execution.

The block-move feature of TI's TMS32020 — up to 80 Mbits per second — allows the large data blocks involved to be accessed in real time to manipulate the screen. The TMS32020 is capable of addressing up to 64K 16-bit words of data used to store the pixel information. Among other features that give the TMS32020 an edge in graphics systems are the scaling shifter used in pixel or bit alignment and the wait states that allow communication with slower DRAMs/VRAMs.

Because a graphics system must interface to a host processor, the host-interface logic on the TMS32020 eases your design task.

TMS32020 simplifies high-speed modem design

Using multiple TMS32020 processors in high-speed modems is a logical choice over costly fully custom chips. The TMS32020 combines easy programming with large data memory, multiprocessor and



serial interfaces, overflow mode, large program memory, and table access of program memory.

Since many high-speed modems require more than one programmable DSP chip, the built-in multiprocessing interface of the TMS32020 minimizes component count and simplifies design.

Adaptive FIR filters require the single-cycle multiply/accumulate/data move and the large data memory of the TMS32020 for high-speed computations and realtime implementation.

The overflow-saturation mode minimizes errors caused by an overflowing accumulator and produces a "clean filter."

Program memory of up to 64K words permits multiple bit rates and standards to be supported simply in software rather than hardware.

For more applications data, call 1-800-232-3200, ext. 3502, or check the coupon on page 4.

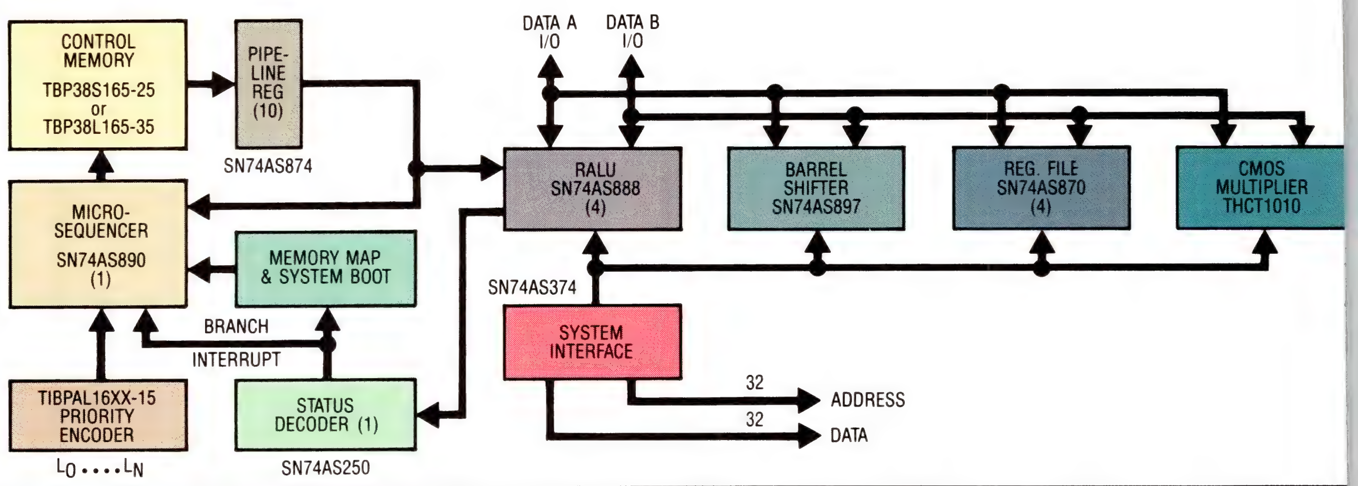
Samples of TI's new 32020 are available now through authorized TI distributors, at $250.* Volume production is slated for early 1986. Development-support tools are also available off the shelf.

TMS32020 Software and Hardware Support

Host Computer	Operating System	Part Number
Macro Assembler/Linkers		
DEC VAX	VMS	TMDS3241210-08
TI/IBM PC	MS-DOS	TMDS3241810-02
Simulators		
DEC VAX	VMS	TMDS3241211-08
TI/IBM PC	MS-DOS	TMDS3241811-02
Hardware		
Emulator		TMDS3262220

*Suggested retail, quantity 1, U.S.A.

Turn the page for more information.



High system performance and low-power operation result when four of TI's new 74AS888 8-bit-slice processors are cascaded to form a 32-bit CPU with TI's new, low-power THCT1010 speeding multiplier/accumulator operations.

TI redefines your idea of speed/power ratios with its new bit-slice/multiplier team.

For many applications requiring exceptional system execution speeds, TI's new 74AS888 8-bit-slice processor can prove the effective alternative to the TMS32020 DSP.

Usually, when you increase system performance significantly, power consumption follows right behind — just as night follows day.

Not so with TI's IMPACT™ 74AS888 and new THCT1010 multiplier/accumulator. This team sends power and performance on their separate ways. One up . . . the other down.

The innovative 74AS888 has an instruction-to-Y output of 46 ns maximum, or a 51% improvement over the 4-bit competition. Power dissipation is only 1.5 W maximum during operation.

Multiplies and divides are about as fast as additions. Flexible microinstructions let you tailor an application-precise instruction set. You can use any software. Any word length in 8-bit increments. Emulate any known μP instruction set while achieving improvements in execution speeds.

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The 74AS888 is fully supported and readily available through TI distributors so you can get your system design finalized in minimum time.

TI's new THCT1010 is pin-for-pin compatible with the industry-standard multiplier (TDC1010J) but consumes 30 times less power. In conjunction with the 74AS888, it can significantly cut the power requirements of bit-slice systems.

Fabricated in silicon-gate CMOS, the THCT1010 is a 16- × 16-bit multiplier with 35-bit accumulator. How fast is it? For the -100 suffix, 100 ns maximum with a worst-case power consumption of only 150 mW.

If you want more details on the 74AS888 and THCT1010, just dial the 800 number below or clip and mail the coupon.

For quick response to your information needs, call Texas Instruments today at **1-800-232-3200.**

27-5287

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Expires June 30, 1986
SPR1Ø3ED5ØØC

YES, please send me the information checked below.

PR22 ☐ TMS32020 Applications Handbook
PR25 ☐ TMS32020 User's Guide
PR12 ☐ TMS32020 Third-party Support
PR3Ø ☐ Digital Signal Processing Newsletter
DBØ1 ☐ IMPACT 74AS888 8-bit-slice Processor Data Sheet and User's Guide
CLØ4 ☐ THCT1010 CMOS Multiplier/Accumulator Data Sheet

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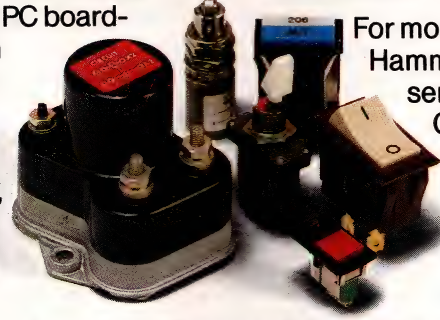

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CIRCLE NO 107

Graphics-controller ICs

Recently introduced graphics-controller ICs offer faster drawing rates and better screen-refresh capabilities than do earlier models. The ICs range from simple screen-refresh controllers to highly specialized 32-bit graphics microprocessors.

Steven H Leibson, *Southwestern Editor*

Recent graphics-controller ICs let you build raster-graphics subsystems that include surprisingly few chips, yet deliver fast drawing speeds previously reached only with bit-slice processors. The ICs also make medium- and low-performance graphics systems easier and less expensive to design and build.

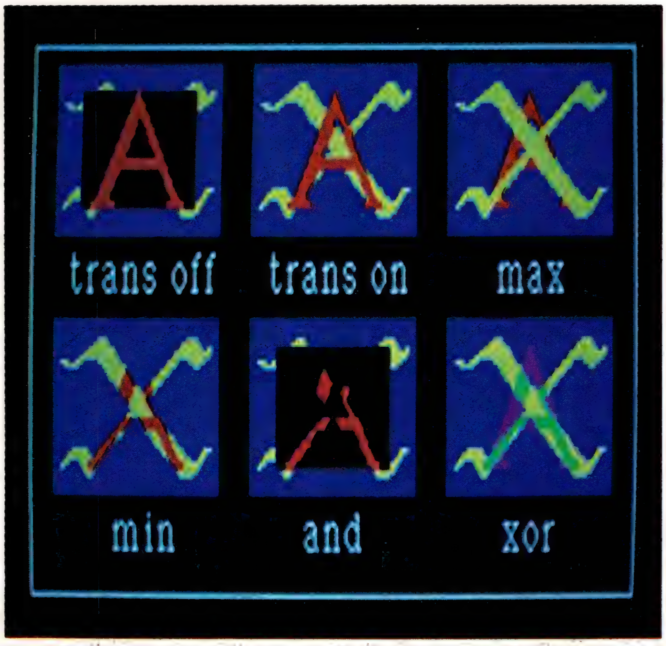
Further, many of these new controllers come with software support for the proposed ANSI Computer Graphics Interface (CGI) standard, which promises standardization at the graphics-driver level for display, hard-copy, and input devices.

Graphics controllers fall roughly into three categories: screen-refresh controllers; fixed-instruction controllers; and application-specific, programmable graphics microprocessors. (High-conversion-rate video D/A converters that work with these different types of controller ICs are listed on pg 116.) Screen-refresh controllers manage CPU access to the screen-buffer RAM, extract display information from the buffer, and direct that information to the CRT-monitor electronics. These controllers also generate CRT

Graphics-controller ICs *offer a variety of approaches to graphics-system design. One chip set, for instance, allows you to approach the construction of a graphics μP in a modular fashion. The set—to be available this spring—includes a raster-graphics processor (which acts as the set's master chip), a BitBlt processing unit, a video clock generator, and a video shift register. For maximum performance, a separate BitBlt processor would manage each memory plane. (Photo courtesy National Semiconductor)*


MEMORY PLANE
VIDEO SHIFT REGISTER DP8515
SLAVE PROCESSOR DP8510
LATCH
DATA
ADDRESS

Any graphics controller that performs screen refresh without the aid of a video RAM cannot draw and refresh at the same time.



Results of several PixBlt operations *combining the letter A and X appear in this screen photo from Texas Instruments' MS-DOS TMS34010 simulator. The results of the operations are, from left to right (top), replacement with transparency off, replacement with transparency on, and maximum. From left to right (bottom), the results are minimum, AND, and Exclusive OR.*

control signals: horizontal and vertical or composite sync and blanking. In designs using screen-refresh controllers, the CPU places the information into the screen buffer (in other words, it draws the picture). Designs using screen-refresh controllers can be inexpensive, but they won't offer very high performance levels because of the great burden they place on the CPU.

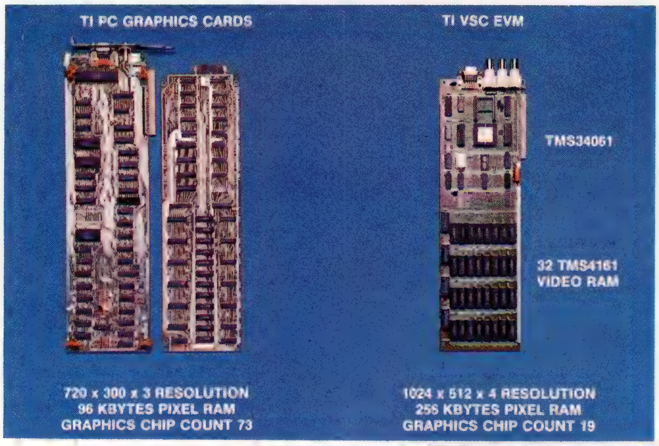
An example of a simple screen-refresh controller is the 6845 NMOS CRT controller from Motorola. IBM uses the device in both the monochrome display and color graphics adapters for the IBM PC family of computers. The 6845 is a character-oriented controller that supports programmable screen formats, including the number of characters displayed both horizontally and vertically, the length of the vertical-retrace period, the width and position of the horizontal sync pulse, and interlace mode. The controller has no onboard character generator.

Although the 6845 is character oriented, you can use it as a screen-timing generator for both character and bit-mapped graphics displays. You can use the 6845's timing signals to drive any screen-buffer architecture. Motorola, Hitachi, VLSI Technology, and Gould AMI offer several NMOS and CMOS versions of the 6845. Both Gould AMI and VLSI Technology offer 6845 macrocells for incorporation into custom IC designs. Fujitsu recently introduced enhanced 6845 designs in CMOS. The company's MB89321 is pin compatible with the 6845; its MB89322 has the same internal architecture, but it has an Intel-type bus interface instead of the 6845's Motorola-type interface. Both parts feature an enhanced, smooth scroll with as many as four independently scrollable screen partitions.

IBM PC-compatible controllers

Specialized screen-refresh controllers for the IBM PC and compatible computers are available from two companies, Chips and Technologies and Tseng Laboratories. The chip sets are compatible with IBM's enhanced graphics adapter card. Chips and Technologies' enhanced graphics chip set comprises the 82C431 graphics controller, the 82C432 sequencer, the 82C433 attributes controller, and the 82C434 CRT controller. These four ICs reduce the chip count of a design compatible with IBM's enhanced graphics adapter from 76 to 32 devices. The chip set supports the IBM PC monochrome display adapter, and it can emulate the Hercules monochrome graphics adapter card.

Tseng Laboratories' ET2000 CRT controller, ET2001 attribute controller, and ET2002 graphics data controller make up a 3-chip set that supports the three screen resolutions (320×200, 640×200, and 640×350 pixels) available with the enhanced graphics adapter. It also supports the additional 640×480-pixel screen format



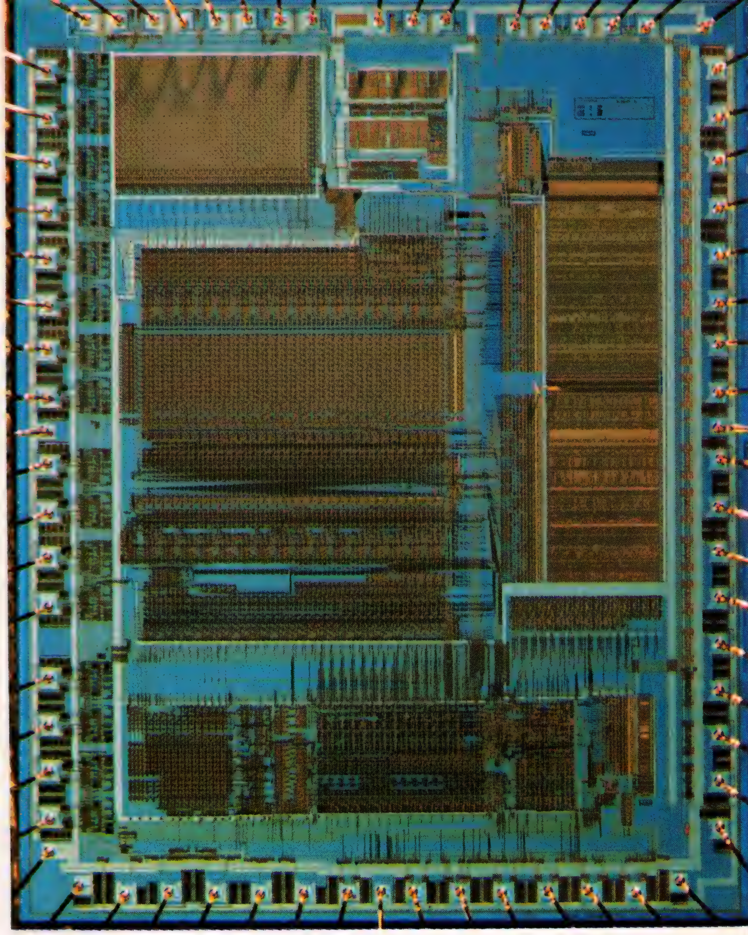
A video-RAM-compatible graphics controller and video RAMs *can reduce board real estate tremendously while increasing maximum screen resolution, as you can see from this comparison of an older, 2-board graphics-board set for Texas Instruments' TI PC bus with the video-system-controller evaluation module.*

available with the IBM Professional graphics controller and the 80-character×25-line screen format of the IBM PC monochrome display adapter. You can build a higher-resolution (1280×1024-pixel) design with one ET2000, one ET2002, and four ET2001s. The company is planning to add a fourth chip to the series: The ET2003 bit-slice controller, for higher-performance subsystems, will be compatible with IBM's Professional graphics controller.

Screen-refresh controllers for bit maps

A screen-refresh controller that specifically addresses bit-mapped graphics is Motorola's raster-memory system, which comprises the MC68486 raster memory interface and the MC68487 raster memory controller. The MC68486 supports from 16k to 1M bytes of screen-buffer RAM. It contains the µP-bus interface, generates system clocks and $\overline{RAS}$ and $\overline{CAS}$ signals for dynamic RAMs, and works in both interlaced and noninterlaced modes.

The MC68487 takes information from the screen buffer and converts it to the video signals needed to drive a display. It supports displays whose resolution is as high as 640×400 pixels for NTSC signals and 640×500 pixels for pal (the French equivalent of NTSC) signals. In character mode, the MC68487 can display as many as 50 rows of 80 characters. The device contains ASCII and block graphics characters in ROM and supports as many as 32,000 user-definable characters. An internal color map allows 32 colors (from a palette of 4096) to appear on the red, green, and blue analog outputs. The video outputs have 100-kΩ output impedance, so you must buffer them externally to drive low-impedance displays.



Suitable for high-performance applications, *this 32-bit, programmable graphics microprocessor, the TMS34010 from Texas Instruments, features a highly parallel architecture, an on-chip instruction cache, and a pixel-block-transfer (PixBlt) raster engine.*

Texas Instruments' TMS34061 video-system controller directly supports 64k-bit video RAMs and display resolutions as high as 4096×4096 pixels. The TMS34061 acts as both a dynamic-RAM controller and a screen-refresh controller: It generates multiplexed addresses, $\overline{RAS}$ and $\overline{CAS}$ signals, the shift-register transfer-

CHARACTER-ORIENTED SCREEN-REFRESH CONTROLLERS

MANUFACTURER	MODEL	NUMBER OF ADDRESS BITS MANAGED (OR ADDRESS SPACE)	NUMBER OF ON-CHIP CHARACTERS	PRICE (QUANTITY)	ALTERNATE SOURCES/NOTES
FUJITSU	MB89321	14	0	\$4.03 (10,000)	PIN COMPATIBLE WITH 6845
	MB89322	14	0	\$4.03 (10,000)	REGISTER COMPATIBLE WITH 6845, INTEL-STYLE BUS INTERFACE
MOTOROLA	6845	14	0	\$6.21 (100)	HITACHI, GOULD AMI, VLSI TECHNOLOGY
SIGNETICS	SAA5350	128k BYTES	512	\$31.59 (100)	CEPT VIDEOTEX A4 TERMINAL CONTROLLER
SMC	CRT9028	2k BYTES	128 PLUS TWO GRAPHIC SETS	\$22.20 (100)	GENERAL INSTRUMENT, INTEL-STYLE BUS INTERFACE
	CRT9128	2k BYTES		\$22.20 (100)	GENERAL INSTRUMENT, MOTOROLA-STYLE BUS INTERFACE
TEXAS INSTRUMENTS	TMS9118A/ TMS9128A/ TMS9129A	16k BYTES	0	\$20.15 (100)	USED IN MSX COMPUTERS
THOMSON-CSF	EF9345	16k	256	\$4 (10,000)	>1000 USER-DEFINABLE CHARACTERS

Video RAMs suit high-performance displays

When they're used as screen buffers for character-oriented displays, where screen manipulation involves only a few thousand bytes, conventional (single-ported) RAMs don't present much of a limitation to system performance. However, bit-mapped displays with resolutions exceeding 1024×1024 pixels have screen buffers of several hundred thousand or millions of bytes, and the limited bandwidth of single-ported RAMs severely degrades the performance of these systems. For high-performance displays, which have large bandwidth requirements for both screen manipulation and screen refresh, you need to use video RAMs.

A video RAM is a 2-port memory device with an internal RAM array and a shift register. One port looks like a conventional dynamic RAM, with multiplexed addresses and $\overline{RAS}$ and $\overline{CAS}$ signals. The other port is serial, coupled to the internal shift register. In one clock, 256 bits (for a 64k-bit video RAM) or 1024 bits (for a 256k-bit video RAM) of data are transferred from the RAM array to the shifter. The serial port then doesn't need the array until the screen-refresh process has used all of the data from the shifter.

Since their introduction a little over a year ago, when Texas Instruments produced the 64k-bit TMS4161, video RAMs have had significant impact on high-performance graphics design. At present, AMD, NEC, and Fujitsu are making 256k-bit video RAMs; TI will soon introduce a 256k-bit device as well. Because the video RAMs have serial ports, they're also finding application in disk, tape, and LAN controllers.

AT&T Technologies' 64k-bit video RAM, the M51064PX, is pin compatible with the TMS4161, although AT&T is not an official alternate source for the TI part. Further, all the 256k-bit video RAMs are pin-compatible, 64k×4-bit designs; however, the NEC μPD41264 offers fewer features than do the other parts listed.

The 256k-bit video RAMs feature bidirectional transfer between the video RAM's shift register and RAM array; you can use this bidirectional transfer for rapid screen clearing and for patterns. In addition, the parts offer maskable write, which lets you use each of a video RAM's four data-signal lines as a separate bit plane, as well as for individual pixel manipulation. You can use the shift-register input for register loading, and you can start shifting at any point in the 256-bit shift register.

VIDEO RAMs

MANUFACTURER	MODEL	RAM-ARRAY CONFIGURATION (BITS)	SHIFTER CONFIGURATION (BITS)	ACCESS TIME (nSEC)	SHIFT RATE (MHz)	PACKAGE	PRICE (QUANTITY)
64k-BIT VIDEO RAMs							
AT&T TECHNOLOGIES	M51064PX-20 M51064PX-15	64k×1 64k×1	256×1 256×1	200 150	16.7 20	20-PIN DIP 20-PIN DIP	$5 (1000)
TEXAS INSTRUMENTS	TMS4161-20 TMS4161-15	64k×1 64k×1	256×1 256×1	200 150	20 22	20-PIN DIP AND 22-LEAD PLCC	$3.20 (100)
256k-BIT VIDEO RAMs							
AMD	Am90C644	64k×4	256×4	100	25	24-PIN, 400-MIL DIP	$10 (1000)
FUJITSU	MB81461-15P MB81461-12P	64k×4 64k×4	256×4 256×4	150 120	16.7 25	24-PIN, 400-MIL DIP AND 24-PIN SIP	$10.75 (10,000) $13 (10,000)
NEC	μPD41264-15 μPD41264-12	64k×4 64k×4	256×4 256×4	150 120	16.7 25	24-PIN, 400-MIL DIP 24-PIN, 400-MIL DIP	$6.90 (100)
TEXAS INSTRUMENTS	TMX4461	64k×4	256×4	120	30	24-PIN, 400-MIL DIP	
HYBRID SIP VIDEO RAMs							
TEXAS INSTRUMENTS	TMS4161EV4 TMS4161EP5 TMS4161GW4 TMS4161GY4	64k×4 64k×5 64k×4 64k×4	256×4 256×5 256×4 256×4	200/150 200/150 200/150 200/150	20/22 20/22 20/22 20/22	31-LEAD SIP 35-LEAD SIP 30-PAD LEADLESS SIP 30-LEAD SIP	$24 (100) $27.20 (100) $24 (100) $24 (100)

*SAMPLES AVAILABLE

An instruction cache accelerates graphics-algorithm execution by capturing loops of instructions.

control signals needed by the video RAMs, and video sync and blank signals. Because screen refresh from video RAMs does not require much RAM bandwidth—and because the TMS34061 performs this screen refresh automatically—you can use one TMS34061 to control both screen-buffer video RAMs and main-system dynamic RAMs. The TMS34061 accepts an 18-bit address from the host CPU and directly drives 64 RAMs. Because the RAM data bus doesn't pass through the TMS34061, the data path between the CPU and memory can be of any width.

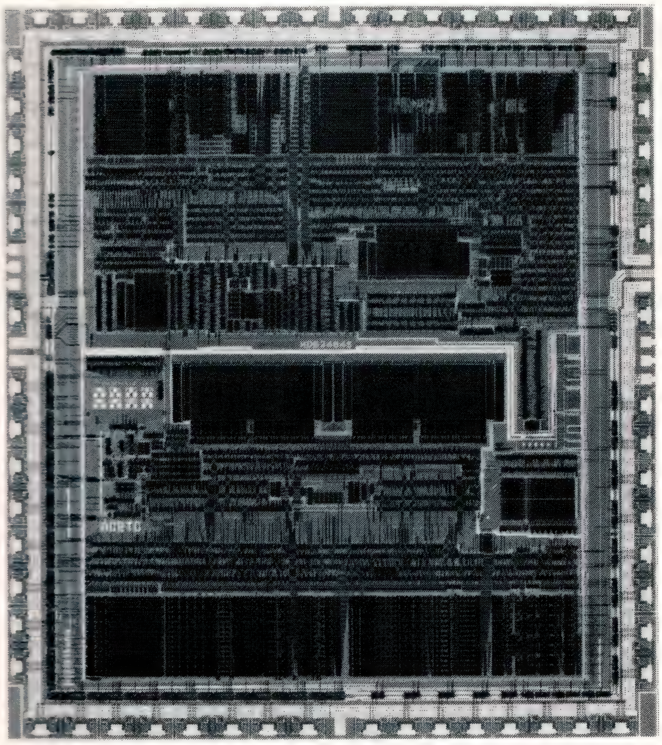
The video-system controller supports both linear and XY-indirect addressing. In the linear-addressing mode, the address presented to the TMS34061 selects a RAM location. This mode is useful primarily in 16- and 32-bit µP systems, which can support the large memory space that a high-resolution screen buffer requires. The XY-indirect addressing mode is useful in systems with 8-bit µPs, which can't support large screen buffers directly. When it operates in the XY-indirect addressing mode, the TMS34061 uses an internally generated 20-bit address to select a RAM location. A programmable automatic increment of the XY-addressing registers supports line-drawing algorithms, so the XY-indirect addressing feature is useful with all CPU types.

An evaluation module for the TMS34061 (the TMDX3471800000) is bus compatible with the IBM PC and the TI PC; it costs $995. The board, which can display a 1024×512-pixel screen, includes a TMS34061 configured with three planes of video RAM. Sockets on the board allow you to add a fourth plane by plugging in eight additional video RAMs.

Another bit-mapped screen-refresh controller is the 82716 video storage and display device from Intel and Matra-Harris, which developed the product jointly. The 82716 has a 512k-byte address space and supports displays that have resolutions as high as 640×512 pixels. You can represent each pixel with two, four, or eight bits (the 8-bit mode is available only for 320-pixel-wide screens). A 16-word color map drives three onboard 4-bit D/A converters, allowing you to display 16 colors from a palette of 4096.

The 82716 directly drives RAM arrays and generates multiplexed addresses and $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$ signals. Standard dynamic RAMs are used for the bit map; the controller generates no transfer or shift control signals for video RAMs. The screen buffer is configured as a 16-bit wide array, and the 82716 offers an 8- or 16-bit interface to the host processor.

A key feature of the 82716 is its window-management scheme. The controller treats windows as objects; it can manage as many as 16 of them. The size and position of each window are determined by two tables: one 512-word access table for all objects and one 8-byte, object-descriptor table for each object displayed. You can program each window to be either bit mapped or character oriented. You control window movement and manipulate window size by altering entries in the relevant tables, a relatively quick operation.

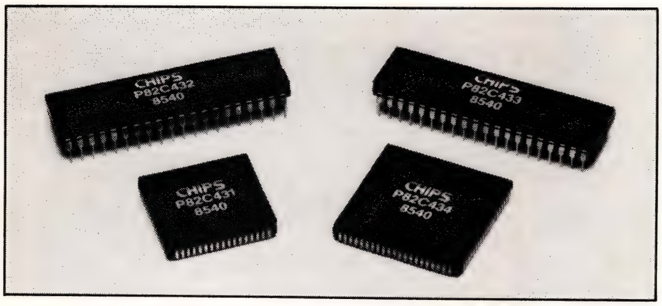


***Graphics, screen-refresh, and RAM-refresh controllers** are combined on the Hitachi HD63484 Advanced CRT controller IC.*

Fixed-instruction controllers

For applications that require higher performance graphics or that must relieve the CPU of graphics tasks, you'll need to use a graphics controller that can manipulate the bit map without CPU intervention. One kind of controller that can perform this task is a fixed-instruction graphics controller, whose fixed instruction sets comprise commands for line and arc drawing.

NEC introduced the first single-chip, fixed-instruction graphics controller, the µPD7220 graphics-display controller. The µPD7220, which is now also offered by Standard Microsystems Corp, Zilog, and Intel, includes screen-refresh, dynamic-RAM refresh, and graphics-



This 4-chip graphics controller *from Chips and Technologies forms the core of a board design that's compatible with the IBM enhanced graphics adapter.*

drawing controllers, as well as a light-pen interface.

The μPD7220's commands include line, arc, rectangle, and graphics-character drawing, which transfers an 8×8-pixel character to designated screen areas and can be used for area fill. Zoom and pan are also supported. NEC's fastest graphics-display controller, the 7220AD-2, clocks at 8 MHz and can draw at 500 nsec/pixel.

A problem with the 7220, as with any graphics controller that refreshes the screen without the aid of a video RAM, is that it can't draw and refresh at the same time. If you allow the graphics controller to draw while the controller is refreshing the screen, snow will appear on the screen when a memory-write cycle (part of the drawing operation) takes the place of the normally scheduled screen-refresh read cycle. One way to prevent snow would be to program the 7220 to draw only during the horizontal and vertical blanking intervals, but the penalty is a severe reduction in drawing speed.

To avoid both snow and slow drawing speed, you could use a screen-refresh controller like the 6845 to relieve the 7220 of its screen-refresh duties. To implement this scheme, you'd use the 7220's external-sync input to synchronize the 7220 with the 6845. This arrangement would require you to use fast RAMs, so you could interleave the drawing cycles and the screen-refresh cycles without extending the overall access time for screen refresh.

However, the main difficulty with this technique is that it requires you to build complex circuitry to detect the 7220's uninterruptible, read-modify-write drawing cycle (which can occur at any time) and postpone the 6845's read cycle until the 7220's cycle is complete.

To overcome this draw-vs-display conflict, Hitachi uses an interleaved memory-access mode in its HD63484-8 advanced CRT controller. A 1000-nsec (at 8 MHz) display/drawing cycle in the interleaved mode provides separate memory cycles for the screen-refresh and drawing tasks. A disadvantage of the interleaved mode is that, for a given screen configuration, the memory-access speed must be twice the speed required by the noninterleaved, single-access mode.

The HD63484-8 controller lets you use 38 drawing commands, including line, rectangle, polyline, polygon, circle, ellipse, arc, ellipse arc, filled rectangle, paint, and pattern. It supports as many as 2M bytes of screen memory with one, two, four, eight, or 16 bits per pixel. The controller also supports a separate 128k-byte character memory space, three split screens, and one window. Signetics will act as an alternate source for the part.

AMD's Am95C60 quad pixel data-flow manager is a

BIT-MAPPED SCREEN-REFRESH CONTROLLERS

MANUFACTURER	MODEL	NUMBER OF ADDRESS BITS MANAGED (OR ADDRESS SPACE)	MAXIMUM SCREEN RESOLUTION (PIXELS)	NUMBER OF BITS OR PLANES PER PIXEL	PRICE (QUANTITY)	ALTERNATE SOURCES/NOTES
AMD	Am8150	18 BITS	N/A	N/A	\$46 (100)	
CHIPS AND TECHNOLOGIES	EGA CHIPSET	256k BYTES	720×350	4	\$85.40/SET (100)	IBM EGA-COMPATIBLE, 4-CHIP SET
INTEL	82716	512k BYTES	640×512	2, 4, OR 8	\$19.95 (10,000)	MATRA-HARRIS
MOTOROLA	MC68486/ MC68487	1M BYTE	640×500 (PAL) 640×400 (NTSC)	1, 2, OR 4	\$20.45 (10,000)	
TEXAS INSTRUMENTS	TMS34061	18 BITS	4096×4096	N/A	\$35.50 (100)	
TSENG LABORATORIES	ET2000 SERIES	256k BYTES/PLANE	1280×1024	8	\$75 PER SET (10,000)	IBM EGA-COMPATIBLE, 3-CHIP SET

Screen-refresh controllers manage CPU access to the screen-buffer RAM, extract display information from the buffer, and direct the information to the CRT.

fixed-instruction graphics controller that takes advantage of video RAMs. One QPDM controls as many as four planes, accessed 16 bits at a time, and supports screen resolutions as high as 4096×4096 pixels. The Am95C60 generates multiplexed addresses and the $\overline{RAS}$ and $\overline{CAS}$ signals needed for dynamic-RAM support, as well as the transfer signal needed for video-RAM control.

By controlling four planes with one chip, AMD implemented an antialiasing algorithm in the Am95C60. The controller performs line smoothing through two or four levels of shading. The Am95C60's 60-instruction command set includes line draw, block move, and area fill. Internally, the Am95C60 is a 16-bit machine, but it supports both 8- and 16-bit interfaces to the host CPU.

The X1001/1002 graphics microprocessor chip set from XTAR Electronics has a display-list architecture. Instead of passing individual drawing instructions to the chip, the CPU interacts with the X1001/1002 by sharing a 128k-byte display-list buffer that's separate from the screen buffer. Using the X1001/1002's display-list-descriptor instruction set, the CPU builds a description (in the buffer) of the picture to be drawn. It then activates the X1001/1002, which runs through the description, executing the instructions, and drawing the picture in a separate frame buffer. The display-list buffer can hold several display lists; if you use an interleaved-access buffer, the host CPU can create a new display list while the X1001/1002 draws from a different, completed list.

The X1001/1002 has no screen-refresh capabilities; you can use either dynamic RAMs or video RAMs as the screen buffer and design your own screen-refresh circuitry. The company incorporates a 6845 screen-refresh controller in its $2195 EVA 1000S evaluation module, however. An IBM PC-compatible video-display board, the PG1000E, costs $3500 and includes a display-list editor; polygon, dither/transparency, and color-palette editors; an assembler; a disassembler; a debugger; and DOS-compatible text drivers.

You can expect several companies to introduce other dedicated graphics microprocessors in 1986. Unlike the X1001/1002, which has a specialized instruction set for drawing, these newer graphics μPs will have general-purpose instruction sets with graphics enhancements in both instruction sets and hardware support.

These high-end machines will employ bit-block transfers (BitBlts) as an efficient means of manipulating the bit map. A BitBlt, which is also called a raster operation (rasterOp), is a primitive graphics operation that takes two rectangular regions of pixels (source and destination), performs a pixel-by-pixel Boolean operation on these blocks, and then writes the resulting block back to the destination.

Because of the BitBlt's Boolean nature, it's mainly suitable for monochrome (one bit per pixel) displays. Texas Instruments has extended the BitBlt operation for multiplane color and gray-scale designs in its TMS34010 graphics system processor by adding arithmetic operations. The company calls the extended function the pixel block transfer (PixBlt).

The TMS34010 (samples of which will be available this month) is based on a 6-MIPS, 32-bit microprocessor core that's like a reduced-instruction-set computer. The

FIXED-INSTRUCTION GRAPHICS CONTROLLERS

MANUFACTURER	MODEL	NUMBER OF ADDRESS BITS MANAGED (OR ADDRESS SPACE)	MAXIMUM SCREEN RESOLUTION (PIXELS)	NUMBER OF BITS OR PLANES PER PIXEL	NUMBER OF COMMANDS	PRICE (QUANTITY)	ALTERNATE SOURCES/ NOTES
AMD	Am95C60	2M BYTES/PLANE	4096×4096	4/95C60	60	*	
HITACHI	HD63484-8	2M BYTES BIT MAP PLUS 128k BYTES TEXT	4096×4096 (AT 1 BIT/PIXEL)	1, 2, 4, 8, OR 16	38	$38.50 (1000)	SIGNETICS
NCR	7300/7301	1M BYTE	1024×1024	2/7301, 8 MAX	25	<$80 (10,000) FOR ONE 7300 AND TWO 7301s	
NEC	7220	512k BYTES	2048×2048 (AT 1 BIT/PIXEL)	1 TO 16	18	$37.50 (100)	INTEL, SMC, ZILOG
THOMSON-CSF	EF9367	64k BYTES/PLANE	1024×512	DETERMINED EXTERNALLY	18	$12 (10,000)	
	EF68483	4M BYTES	2048×2048	4 OR 8	18	**	

*NOT YET AVAILABLE **SAMPLES AVAILABLE

For applications that require higher performance graphics, you'll need a graphics controller that can manipulate the bit map without CPU intervention.

Manufacturers of graphics ICs

For more information on graphics-controller ICs such as the products discussed in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

Advanced Micro Devices
901 Thompson Pl
Sunnyvale, CA 94088
(408) 732-2400
Circle No 678

Analog Devices Inc
Computer Labs Div
Box 280
Norwood, MA 02062
(617) 329-4700
Circle No 679

Analogic Corp
Audubon Rd
Wakefield, MA 01880
(617) 246-0300
Circle No 680

AT&T Technologies Inc
1 Oak Way, Room 2WC-106
Berkeley Heights, NJ 07922
(800) 372-2447
Circle No 681

Brooktree Corp
11175 Flintkote Ave, Bldg F
San Diego, CA 92121
(619) 452-7580
Circle No 682

Chips and Technologies Inc
521 Cottonwood Dr
Milpitas, CA 95035
(408) 434-0600
Circle No 683

Ferranti Electric Inc
87 Modular Ave
Commack, NY 11725
(516) 543-0200
Circle No 684

Fujitsu Microelectronics Inc
Integrated Circuits Div
3320 Scott Blvd
Santa Clara, CA 95054
(408) 727-1700
Circle No 685

General Instrument Corp
Microelectronics Div
600 W John St
Hicksville, NY 11802
(516) 733-3120
Circle No 686

Gould AMI Semiconductors
3800 Homestead Rd
Santa Clara, CA 95051
(408) 246-0330
Circle No 687

Hitachi America Ltd
2210 O'Toole Ave
San Jose, CA 95131
(408) 942-1500
Circle No 688

Honeywell Inc
Signal Processing Technologies
1150 E Cheyenne Mountain Blvd
Colorado Springs, CO 80906
(303) 577-1000
Circle No 689

Inmos Corp
Box 16000
Colorado Springs, CO 80935
(303) 630-4000
Circle No 690

Intech
Microcircuits Div
2270 Martin Ave
Santa Clara, CA 95050
(408) 988-4930
Circle No 691

Intel Corp
3065 Bowers Ave
Santa Clara, CA 95051
(408) 987-8080
Circle No 692

Matra-Harris Semiconducteurs
BP 942 La Chantrerie,
Route de Gachet
44075 Nantes Cedex
France
(40) 303030
Circle No 693

Motorola Semiconductor Products Inc
Box 20912
Phoenix, AZ 85036
(602) 962-2252
Circle No 694

National Semiconductor
2900 Semiconductor Dr
M/S 16-197
Santa Clara, CA 95051
(408) 721-5943
Circle No 695

NCR Corp
Microelectronics Div
1635 Aeroplaza Dr
Colorado Springs, CO 80916
(303) 596-5612
Circle No 696

NEC Electronics Inc
Box 7241
Mountain View, CA 94039
(415) 960-6000
Circle No 697

Pacific Mountain Research Inc
8026 35th Ave NE
Seattle, WA 98115
(206) 524-0910
Circle No 698

Signetics Corp
Box 3409
Sunnyvale, CA 94088
(408) 739-7700
Circle No 699

Silicon Compilers Inc
2045 Hamilton Ave
San Jose, CA 95125
(408) 371-2900
Circle No 700

Standard Microsystems Corp
35 Marcus Blvd
Hauppauge, NY 11788
(516) 273-3100
Circle No 701

Telmos Inc
740 Kifer Rd
Sunnyvale, CA 94086
(408) 732-4882
Circle No 702

Texas Instruments Inc
Box 1443
Houston, TX 77001
(713) 490-2000
Circle No 703

Thomson-CSF Components Corp
301 Rte 17 N
Rutherford, NJ 07070
(201) 438-2300
Circle No 704

Tseng Laboratories Inc
205 Pheasant Run
Newtown Commons, PA 18940
(215) 968-0502
Circle No 705

TRW Electronic Components Group
LSI Products Div
Box 2472
La Jolla, CA 92038
(619) 457-1000
Circle No 706

VLSI Technology Inc
1109 McKay Dr
San Jose, CA 95131
(408) 434-3000
Circle No 707

XTAR Electronics Inc
2262 Landmeier Rd
Elk Grove, IL 60007
(312) 364-4111
Circle No 708

Zilog
1315 Dell Ave
Campbell,CA 95008
(408) 370-8000
Circle No 709

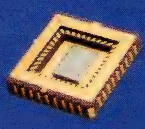
1-chip TMS34010 incorporates a barrel shifter for high-speed bit rotations, and it includes a rasterOp engine, a CRT timing controller, and a video-RAM controller. Local memory can be any combination of video RAM, dynamic RAM, other RAM, and ROM.

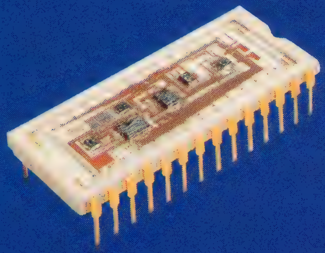
A 256-byte instruction cache is also on chip. The cache accelerates graphics-algorithm execution by capturing loops of instructions. Once a particular instruction loop is captured, memory cycles for instruction fetches within the loop cease, and loop execution is faster, because the TMS34010 can access instruction cache, internal register file, and external memory simultaneously, instead of sequentially. The 256 bytes can hold 128 instructions—an ample capacity for most algorithms.

You can use multiple TMS34010s in your applications

11-Bit Flash Converter

MPS Single Chip . . . vs. . . . Other's Hybrids





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Santa Clara, CA 95054
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CIRCLE NO 69

A fixed-instruction graphics controller can manipulate the bit map without intervention from the CPU.

(for instance, by running several slave TMS34010s from one master). Multiple TMS34010s would suit an application like gun processing, in which each of the three CRT color guns has its own graphics processor.

The TMS34010 supports both linear and XY addressing modes. Linear addressing (the type of addressing available in most general-purpose μPs) is useful for program execution and management of data structures; XY addressing is better for screen and window clipping and other screen-management functions. The TMS34010's 32-bit address architecture can access 4G bits, because the architecture of the part supports bit addressing. The TMS34010 package doesn't bring out the two high-order bits, so the address range is limited to 1G bit.

Fabricated in 1.8-μm CMOS, the TMS34010 graphics microprocessor incorporates 160,000 to 180,000 transistors and dissipates 250 mW at its full rated speed (6 MIPS). Samples cost approximately $500; the company expects to have the part in full production late this year. TI is also planning a line of software-development and -support products for the TMS34010: The products will include low-level, assembly-language tools, a C compiler with a run-time support package, a function library, and support of the CGI standard. You'll be able to select MS-DOS, VMS, Berkeley 4.2 Unix, or Unix System V as the operating system. A software simulator for computers running MS-DOS, as well as a hardware emulator, will also be available.

Motorola plans to introduce a 32-bit graphics microprocessor in the second half of this year. The 68490 raster-graphics display processor is based on a 68000 μP core, but it doesn't support the full 68000 instruction set. Coupled to the processor is a raster engine capable of performing all 16 Boolean operations of a 2-operand rasterOp (source, destination) and all 256 operations of a 3-operand rasterOp (source, mask, destination). The company has not yet determined pricing for the part.

The 68490 supports video RAMs and screen sizes of as much as 1280×1024 pixels with a 16M-bit/plane address space. Without extra hardware, the 68490 can control as many as eight planes. The 68490 doesn't have a built-in screen-refresh controller, so you'll have to include one (such as the 6845) in your subsystem design.

The processor's local memory can comprise any mixture of video RAM, conventional RAM, and ROM. The 68490 has a dual-bus architecture; a host bus interfaces a CPU or DMA controller to the processor. Commands and instructions pass over this bus and through the 68490 into local graphics memory. A program executing in the 68490's local memory then interprets the instructions. You can use the 68490 processor to implement the proposed CGI standard.

This spring, National Semiconductor will introduce its advanced graphics chip set. Comprising the DP8500 raster-graphics processor, DP8510 BitBlt processing unit, DP8512 video clock generator, and DP8515 video shift register, the chip set will allow you to approach the construction of a graphics μP in a modular fashion. The DP8500 and DP8510 are both fabricated in 2-μm CMOS and clock at 20 MHz max. The DP8515, which is fabricated in National's recently announced bipolar/CMOS process, runs as fast as 200 MHz.

The DP8500 is the master chip in the set; it processes instructions from local memory and controls multiple DP8510s. The DP8500 has a 32-bit internal address bus, but, because of pin limitations, it has an external 28-bit address and supports a maximum screen resolution of 16k×16k pixels. The DP8500 has a general-purpose microprocessor core with a full complement of arithmetic and Boolean instructions, and it supports both dynamic RAMs and video RAMs. The DP8500 and its host CPU communicate through shared RAM.

In a maximum-performance configuration of the chip set, each bit plane would be managed by its own DP8510, which contains a rasterOp engine and a barrel shifter. This configuration would support both pixel architecture (manipulation of one bit/plane to the full pixel depth) and plane architecture (manipulation of several adjacent bits in a single plane simultaneously), and you could switch from one orientation to the other from within your program. You could design an architecture that multiplexes one DP8510 over all bit planes, and you could also use the DP8510 as a graphics accelerator for a general-purpose μP even if you had no DP8500 in the system.

The DP8500 is the system address generator; the DP8510s manipulate bit plane data. Allocating a rasterOp processor and barrel shifter to each plane gives the chip set a performance edge over competing single-chip architectures, the company claims.

The DP8512 generates system timing. Although you can use any number of DP8510s in the advanced graphics chip set architecture, the company specifies that both the DP8512 and DP8500 can drive a maximum of eight DP8510s directly. To drive more DP8510s, you would need buffers. An 8-plane system would include one DP8500, one DP8512, and eight DP8510s; these 10

A fixed-instruction graphics controller can manipulate the bit map without intervention from the CPU.

chips would cost about $500. The DP8500 alone costs approximately $200.

The maximum specified pixel clock rate for the DP8512 is 200 MHz. Because that rate outstrips all video-RAM shift rates, National adds a video shift register (the DP8515) to the chip set. A 4-word×16-bit FIFO buffer in the shift register allows for some delay in the video-RAM shifter outputs. This FIFO buffer would be useful in designs that route bit-plane outputs over a backplane to an analog card, the company speculates. **EDN**

Article Interest Quotient (Circle One)
High 470 Medium 471 Low 472

SINGLE VIDEO D/A CONVERTERS

MANUFACTURER	MODEL	RESOLUTION (BITS)	THROUGHPUT (MHz)	COMPATIBILITY	PRICE (QUANTITY)	COMPOSITE INPUTS
ANALOG DEVICES	AD9700	8	125	ECL	$42.50–$74.50 (1)	SYNC, BLANK, REF WHITE, 10% BRIGHT
	AD9768	8	100	ECL	$29.25 (100)	NONE
	HDG-0405	4	150	ECL	$39–$55 (1)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	HDG-0605	6	150	ECL	$44–$64 (1)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	HDG-0805	8	150	ECL	$52–$67 (1)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	HDG-0407	4	50	TTL	$45–$48 (1)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	HDG-0807	8	50	TTL	$55–$61 (1)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
ANALOGIC	AH8308E	8	150	ECL	$45 (100)	SYNC, BLANK, SETUP, 10% BRIGHT
	AH8308T	8	65	TTL	$49 (100)	SYNC, BLANK, SETUP, 10% BRIGHT
	MP8308	8	100 (ECL) 40 (TTL)	ECL OR TTL	$80 (100)	SYNC, BLANK, SETUP, REF WHITE
	MP8318	8	100 (ECL) 40 (TTL)	ECL OR TTL	$77 (100)	NONE
BROOKTREE	Bt102	8	75	TTL/CMOS	$31 (1000)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
FUJITSU	MB40788	10	125	ECL	$63 (10,000)	NONE
	MB40748-8	10 (8-BIT ACC)	20	ECL	$19.80 (10,000)	NONE
	MB40748-9	10 (9-BIT ACC)	20	ECL	$24.39 (10,000)	NONE
	MB40776	6	20	TTL	$7.31 (10,000)	NONE
HONEYWELL SPT	HDAC97000	8	200	ECL	$23 (1000)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
INTECH	VDAC 0405	4	100	ECL	$44 (100)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	VDAC 0605	6	100	ECL	$67 (100)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	VDAC 0805	8	100	ECL	$61 (100)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	VDAC 1840	8	40	TTL/CMOS	$24 (100)	SYNC, BLANK, REF WHITE, 10% BRIGHT
	VDAC 8308THC	8	65	TTL/CMOS	$52 (100)	SYNC, BLANK, SETUP, REF WHITE, 10% BRIGHT
	RGB DAC 3400S	4	40	TTL/CMOS	$40 (100)	SYNC, BLANK, REF RGB
TEKTRONIX	TEK 8120	8	200	ECL	$150 (1)	NONE
	TEK 8121	6	200	ECL	$100 (1)	NONE
	TEK 8130/8131	8	300	ECL	$300 (1)	NONE
TELMOS	TML1840	8	25	TTL	$40–$51 (100)	SYNC, BLANK, 10% BRIGHT
	TML1842	8	25	TTL	$14–$27 (100)	SYNC, BLANK, 10% BRIGHT
	TML1850	8	75–85	TTL	*	SYNC, BLANK, 10% BRIGHT
	TML1852	8	75–85	TTL	*	SYNC, BLANK, 10% BRIGHT
TRW	TDC1012	12	20	TTL	$70 (1000)	NONE
	TDC1112	12	20	ECL	*	NONE
	TDC1018	8	125	ECL	$26 (1000)	SYNC, BLANK, REF WHITE, 10% BRIGHT
	TDC1034	4	125	ECL	$18 (1000)	SYNC, BLANK, 10% BRIGHT

*NOT YET AVAILABLE

Tables continued on pg 118

Your VME system just got faster.

Eleven new VMEbus modules from Dual can make your 32-bit designs take off. Today.

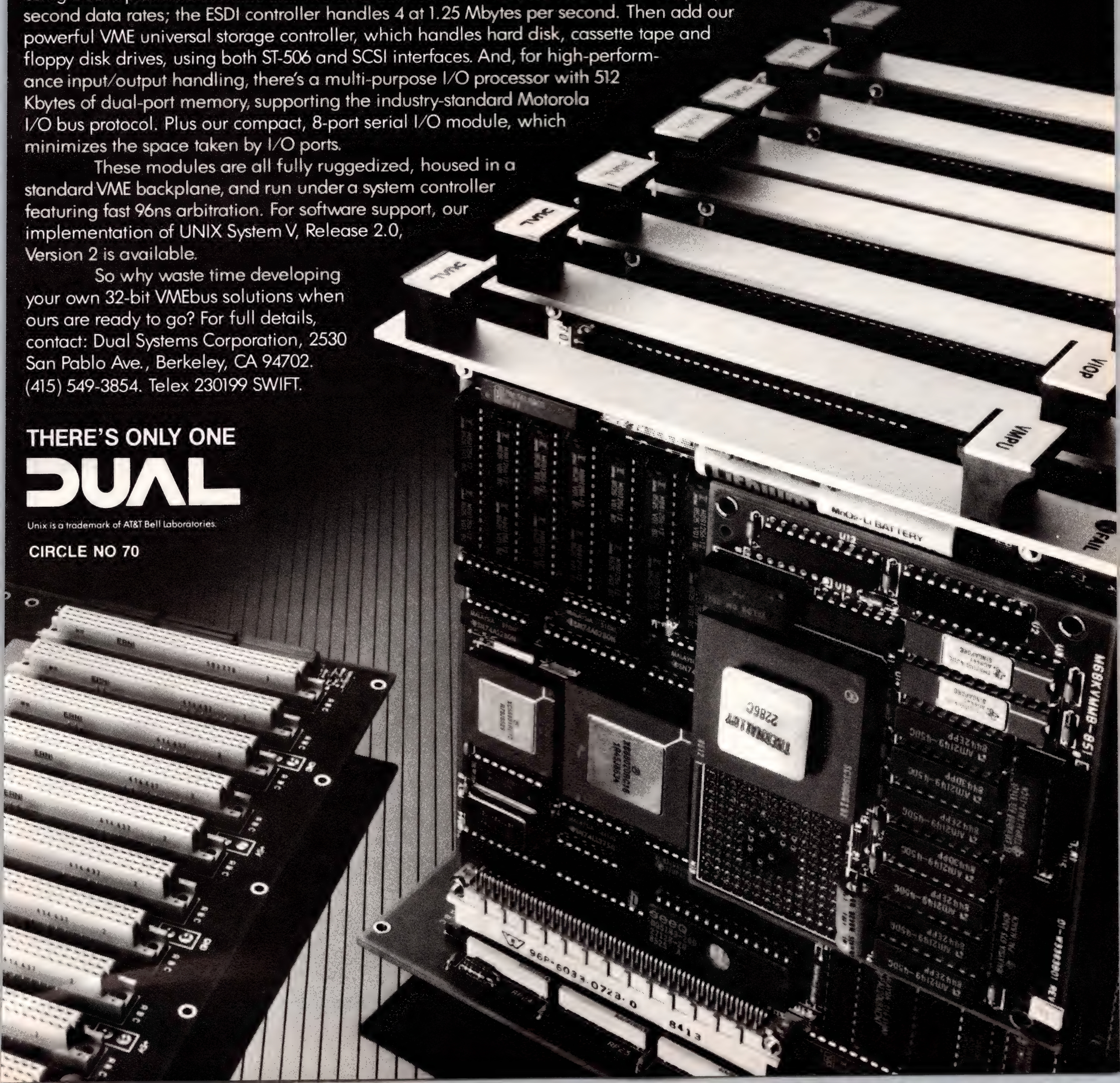
Dual's full line of VMEbus modules is setting new performance and packaging standards in the 32-bit world. Especially among applications that demand high system throughput, fast I/O processing and heavy disk usage.

For performance, start with our multiprocessor engine, the VMPU-32, based on Motorola's advanced MC68020. Optimized for virtual memory UNIX environments, it features extensive interprocessor communication capabilities, a full megabyte of dual-ported local memory, and up to 32 Kbytes of EPROM.

Next, add the industry's fastest, most versatile disk controllers, for both SMD and ESDI formats, using Dual's patented architecture. The SMD controller handles 3 drives with 2.4 Mbyte-per-second data rates; the ESDI controller handles 4 at 1.25 Mbytes per second. Then add our powerful VME universal storage controller, which handles hard disk, cassette tape and floppy disk drives, using both ST-506 and SCSI interfaces. And, for high-performance input/output handling, there's a multi-purpose I/O processor with 512 Kbytes of dual-port memory, supporting the industry-standard Motorola I/O bus protocol. Plus our compact, 8-port serial I/O module, which minimizes the space taken by I/O ports.

These modules are all fully ruggedized, housed in a standard VME backplane, and run under a system controller featuring fast 96ns arbitration. For software support, our implementation of UNIX System V, Release 2.0, Version 2 is available.

So why waste time developing your own 32-bit VMEbus solutions when ours are ready to go? For full details, contact: Dual Systems Corporation, 2530 San Pablo Ave., Berkeley, CA 94702. (415) 549-3854. Telex 230199 SWIFT.



THERE'S ONLY ONE

DUAL

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CIRCLE NO 70

TRIPLE VIDEO D/A CONVERTERS

MANUFACTURER	MODEL	RESOLUTION (BITS/ CHANNEL)	THROUGHPUT (MHz)	COMPATIBILITY	PRICE (QUANTITY)	COMPOSITE INPUTS
ANALOG DEVICES	AD9702	4	125 (ECL) 75 (TTL)	ECL OR TTL	\$50 TO \$63 (1)	SYNC, BLANK, REF WHITE
ANALOGIC	AH8304TC	4	100	TTL	\$49 (100)	SYNC, BLANK
	AH8308TC	8	100	TTL	\$93 (100)	SYNC, BLANK
	AH8308EC	8	150	ECL	\$86 (100)	
	AH8404TC	4	25	TTL	\$52 (100)	SYNC, BLANK
BROOKTREE	Bt101	8	50	TTL/CMOS	\$69 (1000)	SYNC, BLANK, REF WHITE
	Bt103	4	75	TTL/CMOS	\$36 (1000)	SYNC, BLANK
	Bt444	4	40	TTL/CMOS	\$59 (1000)	SYNC, BLANK
FERRANTI	ZN454CJ	4	100	TTL	\$29.76 (100)	RGB SYNC, BLANK
HONEYWELL SPT	HDAC34010	4	200	ECL	\$39 (1000)	SYNC, BLANK, REF WHITE, 10% BRIGHT
	HDAC34020	4	100	TTL	\$39 (1000)	SYNC, BLANK, REF WHITE, 10% BRIGHT
INTECH	VDAC 888E	8	100	ECL	\$149 (100)	SYNC, BLANK
	RGB DAC 3400	4	40	TTL/CMOS	\$58 (100)	SYNC, BLANK, REF RGB
	RGB DAC 3800	8	40	TTL/CMOS	\$90 (100)	SYNC, BLANK, REF AND 10% BRIGHT RGB
	RGB DAC 5151	4	150	TTL OR ECL	\$45 (100)	SYNC, BLANK, REF WHITE, 10% BRIGHT
SIGNETICS	NE5151	4	150	TTL OR ECL	\$43 (100)	SYNC, BLANK, REF WHITE, 10% BRIGHT
TRW	TDC1334	4	100	ECL	\$35 (1000)	SYNC, BLANK, 10% BRIGHT

VIDEO D/A CONVERTERS WITH LOOKUP-TABLE RAM

MANUFACTURER	MODEL	RESOLUTION (BITS/ CHANNEL)	THROUGHPUT (MHz)	COMPATIBILITY	LOOKUP-TABLE RAM SIZE/ CHANNEL (BITS)	PRICE (QUANTITY)	COMPOSITE INPUTS
SINGLE CONVERTERS							
AMD	Am8151	8	200 (ECL) 83.3 (TTL)	ECL OR TTL	256×8	\$40 (100)	HSYNC, VSYNC, BLANK, OVERLAY
TRIPLE CONVERTERS							
ANALOG DEVICES	HDL-3805	8	100	ECL	256×8	\$430 (1)	RGB SYNC, BLANK, REF WHITE, 10% BRIGHT
	HDL-3806	8	100–115	ECL	256×8	\$463–\$512 (1)	RGB SYNC, BLANK, REF WHITE, 10% BRIGHT
ANALOGIC	AH8304TM	4	20	TTL	32×4	\$76 (100)	SYNC, BLANK
	AH8404TM	4	20	TTL	32×4	\$80 (100)	SYNC, BLANK
BROOKTREE	Bt452	4	40	TTL/CMOS	16×4	\$65 (1000)	SYNC, BLANK
	Bt450	4	50	TTL/CMOS	19×4	\$32 (1000)	SYNC, BLANK
	Bt451	4	125	TTL/CMOS	260×4	\$105 (1000)	SYNC, BLANK
INMOS	IMSG170	6	35, 50	TTL	256×6	\$62 (100) (35-MHz VERSION)	SYNC, BLANK
INTECH	RGB DAC 8E	8	100	ECL	256×8	\$434 (100)	RGB SYNC AND BLANK
	RGB DAC 3404	4	40	TTL/CMOS	16×4	\$79 (100)	SYNC, BLANK, REF RGB
	RGB DAC 3405	4	40	TTL/CMOS	32×4	\$121 (100)	BLANK
	RGB DAC 3408	4	40	TTL/CMOS	256×4	\$195 (100)	SYNC, BLANK, REF RGB
	RGB DAC 3808	8	40	TTL/CMOS	256×8	\$184 (100)	SYNC, BLANK, REF AND 10% BRIGHT RGB
	RGB DAC 3405S	4	40	TTL/CMOS	32×4	\$53 (100)	SYNC, BLANK
	RGB DAC 5150	4	80	TTL OR ECL	16×4	\$52 (100)	SYNC, BLANK, REF WHITE, 10% BRIGHT
SIGNETICS	NE5150	4	110	TTL OR ECL	16×4	\$43 (100)	SYNC, BLANK, REF WHITE, 10% BRIGHT
TEXAS INSTRUMENTS	TMS34070	4	36	TTL	16×4	\$24 (100)	BLANK
THOMSON-CSF	EF9369	4	17	TTL	16×4	\$3.50 (10,000)	BLANK

Intelligence, local buses preserve viability of Multibus I

Pacing recent developments in computer architecture, systems based on the 9-year-old Multibus I spec are using subsidiary buses and intelligent I/O boards to offer improved throughput.

Ed Teja, *Western Editor*

Multibus I—a capable, proven architecture for medium-performance computing applications—is known for its flexibility when compared with Q Bus systems and for its power when compared with the STD Bus. But time has its way with all things, including bus architectures: The advent of increasingly powerful microprocessors and the growth of increasingly demanding applications have conspired to force designers to use buses with more power and more capability than the venerable Multibus I can offer. Still, a number of available subsidiary buses and intelligent I/O cards are helping to maintain the viability of the Multibus.

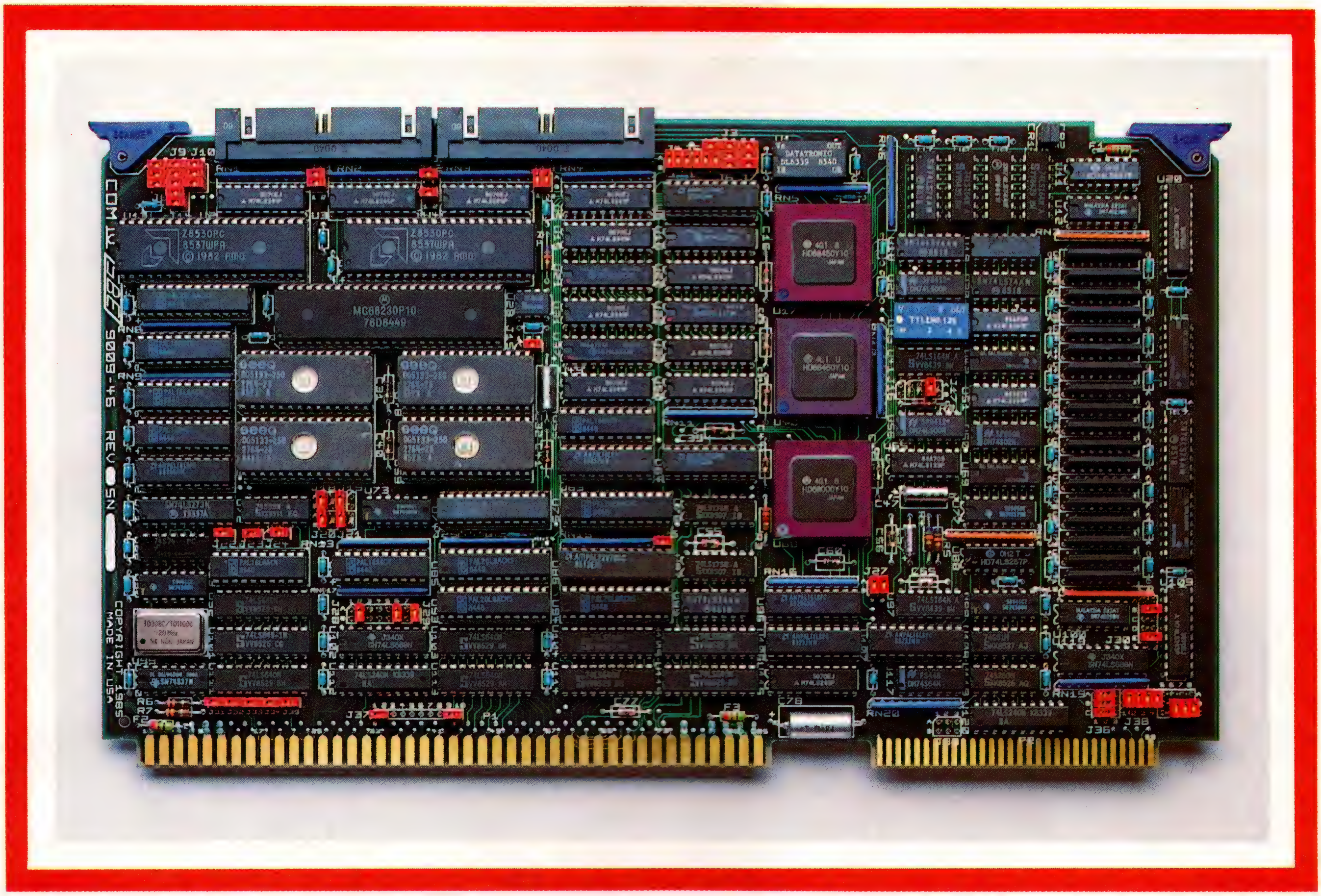
For designers who wish to take advantage of recent developments in computer architecture, but who still intend to base their systems on Multibus I, two inherent limitations cause problems: bus width and bus bandwidth. The 9-year-old Multibus specification won't handle a full 32-bit design. Its 16 data lines and 24 address lines are intended for 8- and 16-bit systems, and it can't directly address the memory required by many of today's system designs. These systems are dominated by the VME Bus and, more recently, Multibus II.

Some CPU board manufacturers, such as Matrox, have seemingly gotten around this limitation of the Multibus I specification by producing 32-bit CPU cards with 16-bit I/O. This strategy is fine if your rationale for moving to 32-bit designs is to take advantage of a particular 32-bit processor's computing power; these boards will provide a solution without requiring a complete system redesign. If you're like most designers, however, you're employing a 32-bit processor to improve overall system performance. The restriction to 16-bit I/O won't render the desired throughput improvement.

Multiprocessing meets bandwidth limits

Another trend in computer architectures is multiprocessing: the division of computational chores among multiple processors. Today, the state of the art in multiprocessing is parallel architecture. Here is where the second limitation of Multibus-based systems comes to bear: Multibus I systems don't have the bandwidth to support sophisticated multiprocessing.

Multiprocessor systems typically place a number of processors on the bus, an arrangement that would overload the Multibus. One approach to resolving these problems has been to resort to multicomputing strate-



On-board intelligence lets sophisticated communications boards, *such as the COM-4 from SBE Inc, relieve the CPU and the Multibus of many communications tasks.*

gies rather than multiprocessing. In a multicomputer environment, the processing chores are shared among multiple computers—transparently to the user.

Subsidiary buses offload CPU

To accommodate multiple computers on the Multibus, you can begin by adding subsidiary I/O buses. Without subsidiary buses, the only path for data, instructions, and addresses is the Multibus itself **(Fig 1a).** The addition of local buses **(Fig 1b)** gives intelligent controllers direct access to dual-ported memory without bothering the CPU. A variety of board products take advantage of these buses to provide system functions, such as data transfers to mass-storage devices, without overloading the Multibus.

Such buses include the iSBX, a low-cost local bus; the iLBX, a high-speed memory bus; and the Multichannel, a high-speed path for block data transfers. These buses provide paths that allow specialized processors to gain access to data stored in the host computer's memory. Intel Corp's iSBX 586 board, for example, implements Ethernet connections. Priced at $600 (100), the board plugs into any host that has an iSBX connector, giving the host an intelligent (82586-based) interface to high-speed communications via a local-area network (LAN) without using Multibus slots. Multiuser operating systems make the system's interaction with the LAN a chore that the CPU doesn't have to deal with.

The next logical step in developing more computer power around the Multibus is to two allow stand-alone computers to share information via other channels. Companies like Mesa Technology Corp (Gaithersburg, MD) provide bus couplers that connect Multibus-based systems to DEC Q Bus or Unibus systems, or even to other Multibus systems.

These boards support DMA transfers between the systems, allowing them to share data without affecting the host system's performance noticeably. The result is the same as having a specialized processor in the same system accessing data via a local bus.

Adding intelligence

The main ingredient in maintaining Multibus I systems' viability, however, is the addition of increasingly powerful Multibus I cards. Sophisticated, intelligent I/O boards, even if they gain access to data through the bus, offload the main processor by reducing the amount of communication required between the CPU and its peripherals. Reducing the necessary communications in turn lowers the bandwidth requirements of the system.

To accommodate multiple computers on the Multibus, you can begin by adding subsidiary I/O buses.

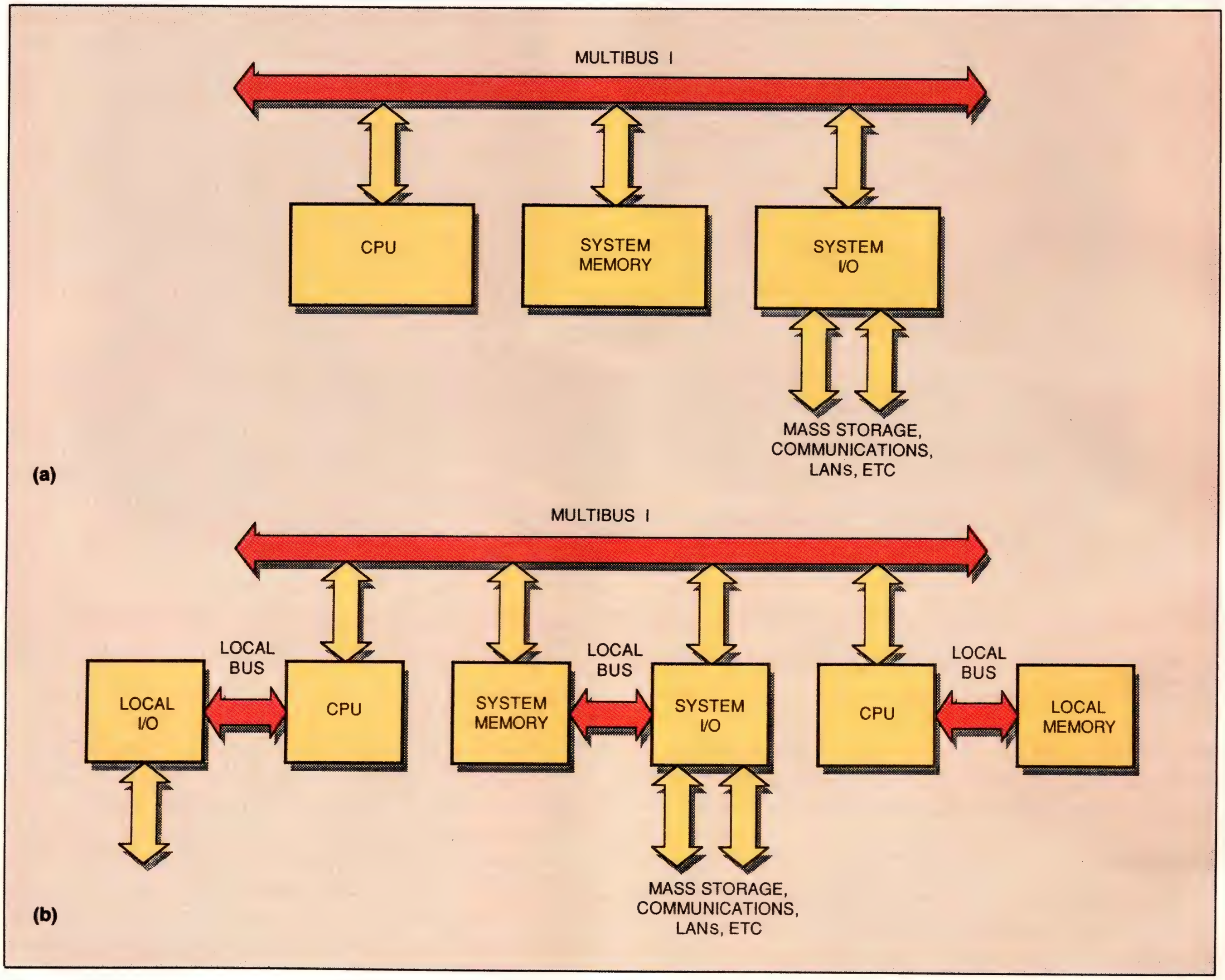


Fig 1—Multibus I provides a narrow pathway *for contemporary system designs **(a)**. Local buses provide paths that allow intelligent I/O modules to share data without loading down the main bus **(b)**.*

In the graphics field, for example, companies such as Datacube provide video acquisition, storage, processing, and display capabilities on Multibus cards. Datacube's VG-124 displays 640×256 pixels in 64 gray levels, and it features scroll, zoom, and high/low resolution. Boards like these let you add graphics capability without bogging down system performance.

Certainly, these I/O systems do nothing to alleviate the inability of Multibus I to accommodate 32-bit-wide data transfers, but they do offer performance increases that let you fabricate systems competitive with their 32-bit kin in certain market niches.

As a result of the inherent bus-width and bandwidth limitations, Multibus I systems tend to grow outward: These intelligent I/O boards expand a Multibus system so that it can meet the needs of the application they serve. The I/O boards provide a system growth path, whether it is toward more and faster mass storage or toward interaction with other computer systems.

The definition process

For the purposes of this directory, we've grouped the boards into two large categories: data controllers and mass-storage controllers. The tables include only full Multibus I boards. We've elected to exclude iSBX and other subsidiary buses, which would serve to confuse rather than complement this directory.

The data-controller category (**Table 1**, pg 124) in-

cludes such communications boards as serial I/O, parallel I/O, and analog I/O. **Table 2** (pg 128) lists Multibus I mass-storage controller cards. You'll see that multifunction controllers are the mass-storage equivalents of intelligent I/O cards. These boards handle a variety of tape and disk devices rather than simply floppy or Winchester disk drives. Industry analyst Joe Jaworski, president of Peripheral Concepts (Irvine, CA), expects that 43.2% of all controllers will support multiple devices by 1988 **(Ref 1)**. These controllers are changing primarily to meet the needs of CAD/CAM workstations, which represent the leading edge of affordable high-performance computer systems.

Use this directory as a starting point to determine the features you can give your system. The board vendors listed will be delighted to tell you of the piggyback boards and other options that can extend a system's functionality even further. **EDN**

Reference

1. *1985 Controller Concepts,* Vol 2, Peripheral Concepts Inc, 18003-G2 Skypark Circle, Irvine, CA 92714. Phone (714) 250-9510.

Article Interest Quotient (Circle One)
High 473 Medium 474 Low 475

For more information . . .

For more information on the Multibus I/O boards described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Aviv Corp
26 Cummings Park
Woburn, MA 01801
(617) 933-1165
Circle No 645

Burr-Brown Corp
Box 11400
Tucson, AZ 85734
(602) 746-1111
Circle No 646

Central Data Corp
1602 Newton Dr
Champaign, IL 61820
(217) 359-8010
Circle No 647

Ciprico Inc
2955 Xenium Lane
Plymouth, MN 55441
(612) 559-2034
Circle No 648

Comark Corp
93 West St
Medfield, MA 02052
(617) 359-8161
Circle No 649

Communications Machinery Corp
1421 State St
Santa Barbara, CA 93101
(805) 963-9471
Circle No 650

Datacube Inc
4 Dearborn Rd
Peabody, MA 01960
(617) 535-6644
Circle No 651

Data Technology Corp
2775 Northwestern Pkwy
Santa Clara, CA 95051
(408) 496-0434
Circle No 652

Datel
11 Cabot Blvd
Mansfield, MA 02048
(617) 339-9341
Circle No 653

E F Data Corp
1233 N Stadem Dr
Tempe, AZ 85281
(602) 968-0447
Circle No 654

Intel Corp
5200 NE Elam Young Pkwy
Hillsboro, OR 97123
(503) 640-7157
Circle No 655

Interphase Corp
2925 Merrel Rd
Dallas, TX 75229
(214) 350-9000
Circle No 656

Konan Corp
1425 N 27th Ave
Phoenix, AZ 85009
(602) 269-2649
Circle No 657

Matrox Electronic Systems Ltd
1055 St Regis Blvd
Dorval, Quebec, Canada H9P2TP
(514) 685-2630
Circle No 658

Metacomp Inc
9466 Black Mountain Rd
San Diego, CA 92126
(619) 578-9840
Circle No 659

Microbar Systems Inc
785 Lucerne Dr
Sunnyvale, CA 94086
(800) 821-1011; in CA, (800) 421-1752
Circle No 660

Mini Computer Technology
696 E Trimble Rd
San Jose, CA 95131
(408) 942-1616
Circle No 661

Morrow Technologies Corp
3026 Owen Dr
Antioch, TN 37013
(615) 793-3555
Circle No 662

Omnibyte Corp
245 W Roosevelt Rd
West Chicago, IL 60185
(312) 231-6880
Circle No 663

Plessey Microsystems
1 Blue Hill Plaza
Pearl River, NY 10965
(800) 368-2738; in NY, (914) 735-4661
Circle No 664

Proteon Inc
4 Tech Circle
Natick, MA 01760
(617) 655-3340
Circle No 665

Qualogy Inc
2241 Lundy Ave
San Jose, CA 95131
(408) 946-5800
Circle No 666

SBE Inc
2400 Bisso Lane
Concord, CA 94520
(800) 221-6450;
in CA, (800) 328-9900
Circle No 667

Scientific Micro Systems
339 N Bernardo
Mountain View, CA 94048
(415) 964-5700
Circle No 668

Systech Corp
6465 Nancy Ridge Rd
San Diego, CA 92121
(619) 453-8970
Circle No 669

Wespercorp
14511 New Myford Rd
Tustin, CA 92680
(714) 730-6250
Circle No 670

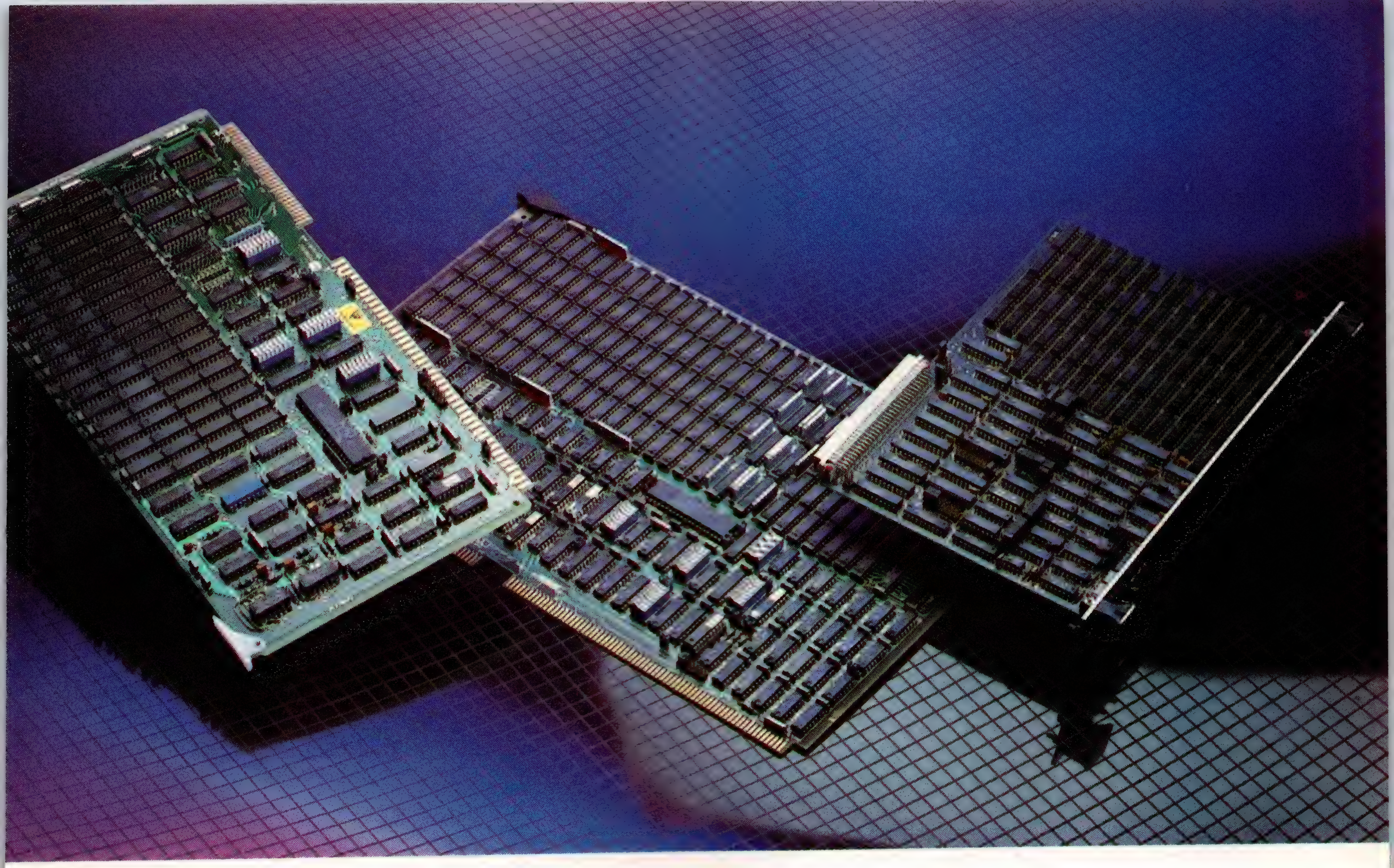
Xylogics
144 Middlesex Tpke
Burlington, MA 01803
(617) 272-8140
Circle No 671

Zendex Corp
6700 Sierra Lane
Dublin, CA 94568
(415) 828-3000
Circle No 672

TABLE 1—MULTIBUS I I/O BOARDS

VENDOR	MODEL	TYPE	NUMBER OF SERIAL CHANNELS	MAX BAUD RATE	NUMBER OF PARALLEL LINES	PRICE	COMMENTS
BURR-BROWN CORP	MP801	DIGITAL OUTPUT BOARD	0	N/A	16	$325 (1 TO 49)	RELAY OUTPUT SYSTEM
	MP802	DIGITAL OUTPUT BOARD	0	N/A	32	$495 (1 TO 49)	RELAY OUTPUT SYSTEM
	MP810	DIGITAL INPUT BOARD	0	N/A	24	$450 (1 TO 49)	
	MP8304	D/A CONVERTER	4-CHANNEL D/A CONVERTER, 8 DIFFERENTIAL CHANNELS, 16 SINGLE-ENDED CHANNELS	N/A	0	$775 (1 TO 49)	
	MP8418	ANALOG I/O	2 OUTPUT, 32 INPUT	N/A	0	$740 (1 TO 49)	12-BIT RESOLUTION
	MP8632	ANALOG I/O	2 OUTPUT, 64 SINGLE-ENDED	N/A	0	$535 (1 TO 49)	8-BIT RESOLUTION
CENTRAL DATA CORP	B1031	SERIAL I/O	8	19.2k	0	$705 (100)	BASED ON AN 8088; INCLUDES 64k-BYTE BUFFER
COMMUNICATION MACHINERY CORP	DNP-30	LAN BOARD	1	10M	0	$2300	SUPPORTS TCP/IP AND X.25 PROTOCOLS
DATEL	ST-701	ANALOG-TO-DIGITAL	16 SINGLE-ENDED OR 32 DIFFERENTIAL	N/A	0	$1170 TO $1585	CHOICE OF 12-, 14-, OR 16-BIT RESOLUTION
	ST-702	ANALOG-TO-DIGITAL	8	N/A	0	$1095	FOR THERMO-COUPLE INPUTS; 13-BIT RESOLUTION/ 128-dB CMRR
E F DATA CORP	BCM-201	MODEM BOARD	1	2.5M	0	$780 (25 TO 50)	WORKS WITH COAXIAL LANs
INTEL CORP	iSXM MAP COMMENGINE	COMMUNICATIONS BOARD	1	10M	0	$3750	SUPPORTS MAP PROTOCOL; INCLUDES 256k BYTES OF RAM
	iSBC 188/56	COMMUNICATIONS BOARD	8 (EXPANDABLE TO 12)	19.2k	0	$1895	SUPPORTS ASYNC, BISYNC, HDLC, AND SDLC PROTOCOLS
	iSBC 88/45	COMMUNICATIONS BOARD	3	19.2k	0	N/A	SUPPORTS RS-232C, CCITT V.24, AND RS-422A/449
MATROX ELECTRONIC SYSTEMS LTD	CP2000	COMMUNICATIONS PROCESSOR	8	19.2k	0	$2495	INCLUDES ETHERNET (802.3) CHANNEL
METACOMP INC	MSC-1062	SERIAL I/O	8	76.8k	0	$975 (50)	BASED ON AN 8088; INCLUDES 128k-BYTE BUFFER
	MPA-2160	SERIAL I/O	16	76.8k	0	$2925 (50)	INCLUDES 128k-BYTE BUFFER; JUMPER-SELECTABLE DTE OR DCE

VENDOR	MODEL	TYPE	NUMBER OF SERIAL CHANNELS	MAX BAUD RATE	NUMBER OF PARALLEL LINES	PRICE	COMMENTS
MICROBAR SYSTEMS INC	COM16	COMMUNICATIONS BOARD	8 ON BASIC SYSTEM (EXPANDABLE TO 16)	56k	0	$1890	EXPANDABLE BUFFER MEMORY TO 512k BYTES
MORROW TECHNOLOGIES CORP	MX-422	COMMUNICATIONS CONTROLLER	8	76.8k	0	$895 (100)	FEATURES OPTIONAL TRANSIENT SUPPRESSION
OMNIBYTE CORP	OB68K/INT (S)	SERIAL I/O	4	38.4k	0	$695	
	OB68K/OCTAL	SERIAL I/O	8	38.4k	0	$795	
	OB68K/INT (P)	PARALLEL I/O	0	N/A	48	$495	INCLUDES SASI AND CENTRONICS PRINTER INTERFACES
	OB68K/230	PARALLEL I/O	0	N/A	96	$395	
PLESSEY MICROSYSTEMS	IOP-1	SERIAL I/O	8	19.2k	N/A	$1988	16k-BYTE BUFFER; 8086-BASED
PROTEON INC	P1200	LAN BOARD	1	10M	0	$3150	SUPPORTS PROPRIETARY TOKEN-PASSING LAN
	P1280	LAN BOARD	1	80M	0	$8000	SUPPORTS PROPRIETARY TOKEN-PASSING LAN
SBE INC	COM-4	COMMUNICATIONS BOARD	4	3M	0	$1195 (100)	INCLUDES TWO DMA CHANNELS; SUPPORTS SDLC, HDLC, X.25, AND BISYNC
	COM-II	COMMUNICATIONS BOARD	2	3M	0	$1295 (100)	SUPPORTS SDLC, HDLC, X.25, AND BISYNC
	M68COM	COMMUNICATIONS BOARD	8	38.4k	0	$1175 (100)	SUPPORTS SDLC, HDLC, X.25, AND BISYNC
SYSTECH CORP	DCP-8804	SERIAL I/O	4	1M	0	$1675 TO $2365 (100)	INCLUDES TWO DMA CHANNELS AND A 64k- TO 512k-BYTE BUFFER
ZENDEX CORP	ZX-514	SERIAL I/O	4	19.2k	0	$200 (100)	
	ZX-515	SERIAL I/O	5	19.2k	0	$525 (100)	
	ZX-560	PARALLEL I/O	0	N/A	72	$420 (100)	
	ZX-572	PARALLEL I/O	0	N/A	72	$500 (100)	ORGANIZED AS NINE 8-BIT PORTS
	ZADC-518	COMMUNICATIONS BOARD	8	56k	0	$2100 (100)	SUPPORTS HDLC, SDLC, AND X.25 PROTOCOLS



A Few Intimate Questions to Ask Your Supplier Before You Buy Your Next System Bus Boards:

1. Who really builds the boards?
Your supplier may not be building them . . . just selling them. Find out. Job shop quality can be risky business.

2. Is the production facility good enough to meet U.S. and U.K. mil specs?
Unless it's Plessey Microsystems, the answer is no. Only Plessey produces each and every board in a facility which meets U.S. (AQAP 1&2) and U.K. (DEF. STAN. 05-21) military specifications for production . . . giving you military quality at commercial prices.

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TABLE 2—MULTIBUS I MASS-STORAGE CONTROLLER CARDS

			DRIVE CHARACTERISTICS			
MANUFACTURER	**MODEL NUMBER**	**CONTROLLER TYPE**	**DRIVE INTERFACE**	**MAXIMUM NUMBER OF DRIVES**	**SECTOR SIZES** (BYTES)	**ERROR DETECTION**
AVIV CORP	TFC 505	TAPE ONLY (9 TRACKS)	PERTEC/STC	4 TAPE DRIVES	TO 64k	N/A (IN THE FORMATTER)
CENTRAL DATA CORP	CD21/4029	TAPE ONLY (¼-IN. CARTRIDGE)	QIC-02	4 TAPE DRIVES	512	N/A (IN THE FORMATTER)
	CD21/4300	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506 (WINCHESTER), SA850/450 (FLOPPY), QIC-02 (TAPE)	4 WINCHESTERS, 4 TAPES, 4 FLOPPIES	128 THROUGH 1k	32-BIT ECC
CIPRICO INC	PICO-MATE	TAPE ONLY (¼-IN. CARTRIDGE)	KENNEDY 6455	2 TAPE DRIVES	N/A	N/A (IN THE FORMATTER)
	TAPEMASTER A	TAPE ONLY (9 TRACKS)	PERTEC	8 TAPE DRIVES	TO 64k	N/A (IN THE FORMATTER)
	RIMFIRE 44A	MULTIFUNCTION (WINCHESTER/TAPE)	ANSI BSR X3.101 (DISK), QIC-02 (TAPE)	8 WINCHESTERS, 4 TAPES	128 THROUGH 1k	32-BIT ECC
	RIMFIRE 45A	MULTIFUNCTION (WINCHESTER/TAPE)	ANSI BSR X3.101 (DISK), PERTEC (TAPE)	8 WINCHESTERS, 4 TAPE DRIVES	128 THROUGH 1k	N/A
	RIMFIRE 50	WINCHESTER ONLY (8- OR 14-IN.)	SMD (1.8M BYTES/SEC)	4 WINCHESTERS	PROGRAM-MABLE	48-BIT ECC
	TAPEMASTER 1000	TAPE ONLY (9 TRACKS)	PERTEC	8 TAPE DRIVES	TO 64k	N/A (IN THE FORMATTER)
	RIMFIRE 1200	WINCHESTER ONLY (8- OR 14-IN.)	SMD (2.5M BYTES/SEC)	4 WINCHESTERS	PROGRAM-MABLE	48-BIT ECC
	RIMFIRE 75T	TAPE ONLY (¼-IN. CARTRIDGE)	3M HCD-75	4 TAPE DRIVES	N/A	N/A (IN THE FORMATTER)
	QUARTER-MASTER	TAPE ONLY (¼-IN. CARTRIDGE)	QIC-02	4 TAPE DRIVES	512 BYTES	N/A (IN THE FORMATTER)
COMARK CORP	MT80	TAPE ONLY (9 TRACKS)	PERTEC	8 TAPE DRIVES	TO 2k	N/A (IN THE FORMATTER)
	MT86	TAPE ONLY (9 TRACKS)	PERTEC	8 TAPE DRIVES	TO 65k	N/A (IN THE FORMATTER)
	MF85	FLOPPY ONLY (5¼- OR 8-IN.)	SA850/460	FOUR 8-IN. AND THREE 5¼-IN. FLOPPIES	PROGRAM-MABLE	N/A
DATA TECHNOLOGY CORP	5186	WINCHESTER ONLY (5¼-IN.)	ST506	2 WINCHESTERS	128 THROUGH 1k	32-BIT ECC
	5286	MULTIFUNCTION (WINCHESTER/FLOPPY)	ST506 (WINCHESTER), SA450 (FLOPPY)	2 WINCHESTERS, 2 FLOPPIES	128 THROUGH 1k	32-BIT ECC
	5486	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506 (WINCHESTER), SA450 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 CARTRIDGE TAPE	128 THROUGH 1k	32-BIT ECC

		HOST CHARACTERISTICS					
ERROR CORRECTION	**FLAW SKIPPING**	**SUPPORT LEVEL**	**SIZE OF BUFFER** (BYTES)	**HOST TRANSFER RATE**	**MINIMUM INTERLEAVE**	**OEM PRICE** (US)	**COMMENTS**
N/A (IN THE FORMATTER)	BLOCK REWRITES	24-BIT ADDRESSING	4k (32k OPTIONAL)	2.5M BPS	N/A	$3800	TRIDENSITY TAPE COUPLER TO 200-IPS SPEEDS
N/A (IN THE FORMATTER)	BLOCK REWRITES	D8/M24 (MASTER)	NONE	N/A	N/A	$310	ONBOARD DMA
11-BIT BURST	TRACK LEVEL	D16/M24 (MASTER)	2k (STD), 8k (OPTIONAL)	10M BPS	1:1	$1300	OPTIMIZED FOR UNIX, ONBOARD CACHE, OPTIONAL iLBX DMA INTERFACE
N/A (IN THE FORMATTER)	N/A	24-BIT ADDRESSING	NONE	N/A	N/A	$1190	TAPEMASTER COMPATIBLE, ½-IN. TAPE EMULATION
N/A (IN THE FORMATTER)	BLOCK REWRITES	24-BIT ADDRESSING	4 TO 16k (OPTIONAL)	N/A	N/A	$1790	TRIDENSITY TAPE COUPLER START/STOP OR STREAMING
5-BIT BURST	N/A	24-BIT ADDRESSING	NONE	N/A	N/A	$1995	AUTO-BACKUP/RESTORE
N/A	N/A	24-BIT ADDRESSING	NONE	N/A	N/A	$2095	
16-BIT BURST	N/A	24-BIT ADDRESSING	8 TO 32k (OPTIONAL)	N/A	N/A	$1775	
N/A (IN THE FORMATTER)	BLOCK REWRITES	24-BIT ADDRESSING	1k (4k OPTIONAL)	4M BPS	N/A	$1890	TRIDENSITY TAPE COUPLER; TAPE SPEEDS TO 1.5M BPS
16-BIT BURST	N/A	24-BIT ADDRESSING	32k CACHE	N/A	1:1	$2195	
N/A (IN THE FORMATTER)	BLOCK REWRITES	24-BIT ADRESSING	N/A	N/A	N/A	$995	ONBOARD BACKUP AND RESTORE
N/A (IN THE FORMATTER)	BLOCK REWRITES	24-BIT ADDRESSING	NONE	N/A	N/A	$550	
N/A (IN THE FORMATTER)	BLOCK REWRITES	ONBOARD DMA	1k (8k OPTIONAL)	N/A	N/A	$895	COUPLER FOR NRZ/PE TAPE DRIVES, TO 125-IPS SPEEDS
N/A (IN THE FORMATTER)	BLOCK REWRITES	24-BIT DMA	N/A	N/A	N/A	$895	COUPLER FOR NRZ/PE TAPE DRIVES, TO 125-IPS SPEEDS
N/A	N/A	20-BIT ADDRESSING	NONE	N/A	N/A	$695	SUPPORTS DOUBLE-SIDED, DOUBLE-DENSITY FLOPPIES; HAS ONBOARD MATH PROCESSOR
11-BIT BURST	TRACK LEVEL	8/16 DATA, 16/20/24 ADD	N/A	1.6M BPS	1:1	$495	
11-BIT BURST	TRACK LEVEL	8/16 DATA, 16/20/24 ADD	N/A	1.6M BPS	PROGRAM-MABLE	$620	
11-BIT BURST	TRACK LEVEL	8/16 DATA, 16/20/24 ADD	16k	1.6M BPS	1:1	$780	

Table continued on pg 130

TABLE 2—MULTIBUS I MASS-STORAGE CONTROLLER CARDS *(continued)*

MANUFACTURER	MODEL NUMBER	CONTROLLER TYPE	DRIVE CHARACTERISTICS: DRIVE INTERFACE	MAXIMUM NUMBER OF DRIVES	SECTOR SIZES (BYTES)	ERROR DETECTION
INTEL CORP	iSBC 226	WINCHESTER ONLY (8- OR 14-IN.)	SMD (2M BYTES/SEC)	2 WINCHESTERS	1024 ONLY	32-BIT ECC
	iSBC 220	WINCHESTER ONLY (8- OR 14-IN.)	SMD	4 WINCHESTERS	128 THROUGH 1k	32-BIT FIRE CODE
	iSBC 208	FLOPPY ONLY (5¼- OR 8-IN.)	SA850/400	4 FLOPPIES	256 THROUGH 4k	N/A
	iSBC 214	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506 (WINCHESTER), SA450 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 4 FLOPPIES, 4 TAPES	128 THROUGH 1k	32-BIT ECC
	iSBC 215G	WINCHESTER ONLY (5¼-IN.)	ST506	2 WINCHESTERS	PROGRAM-MABLE	32-BIT ECC
	iSBC 215	WINCHESTER ONLY (5¼-, 8, OR 14-IN.)	ANSI X379/1226	4 WINCHESTERS	128 THROUGH 1k	32-BIT ECC
INTERPHASE CORP	SDC 2203	FLOPPY ONLY (5¼- OR 8-IN.)	SA850/460	4 FLOPPIES	256 THROUGH 1k	N/A
	WDC 2881	WINCHESTER ONLY (8-IN.)	ANSI	4 WINCHESTERS	PROGRAM-MABLE	32-BIT ECC
	SMD 2181	WINCHESTER ONLY (8- or 14-IN.)	SMD (2.4M BYTES/SEC)	4 WINCHESTERS	PROGRAM-MABLE	32-BIT ECC
	SMD 2180	WINCHESTER ONLY (8- OR 14-IN.)	SMD	4 WINCHESTERS	128, 256, OR 512	ECC
	STORAGER	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506/412HP/ESDI (WINCHESTER), SA460 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 2 TAPE DRIVES	128 THROUGH 1k	32-BIT ECC
	SMD 2190	WINCHESTER ONLY (8- OR 14-IN.)	SMD (2.4M BYTES/SEC)	4 WINCHESTERS	PROGRAM-MABLE	32-BIT ECC
KONAN CORP	TAISHO 6000	MULTIFUNCTION (WINCHESTER/ FLOPPY)	ST506 (WINCHESTER), SA850/450 (FLOPPY), FLOPPY TAPE	4 WINCHESTERS, 4 FLOPPIES, OR 1 FLOPPY AND 1 FLOPPY TAPE	128, 256, OR 512	CRC
MINI COMPUTER TECH	MCT 4300	WINCHESTER ONLY (8- OR 14-IN.)	SMD	4 WINCHESTERS	PROGRAM-MABLE	16-BIT CRC
	MCT 4500	WINCHESTER ONLY (5¼- OR 8-IN.)	SA1000/ST506	4 WINCHESTERS	PROGRAM-MABLE	32-BIT ECC
	MCT 4510	MULTIFUNCTION (WINCHESTER/TAPE)	ST506, QIC-02	3 WINCHESTERS, 4 CARTRIDGE TAPES	PROGRAM-MABLE	32-BIT ECC
QUALOGY	MICRO-CHARGE 5214	MULTIFUNCTION (WINCHESTER/FLOPPY)	ST506 (WINCHESTER), SA450 (FLOPPY)	2 WINCHESTERS, 2 FLOPPIES	128 THROUGH 1k	32-BIT ECC
	RAMTRAC 5217B	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506 (WINCHESTER), SA450 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 TAPE	128 THROUGH 1k	32-BIT ECC

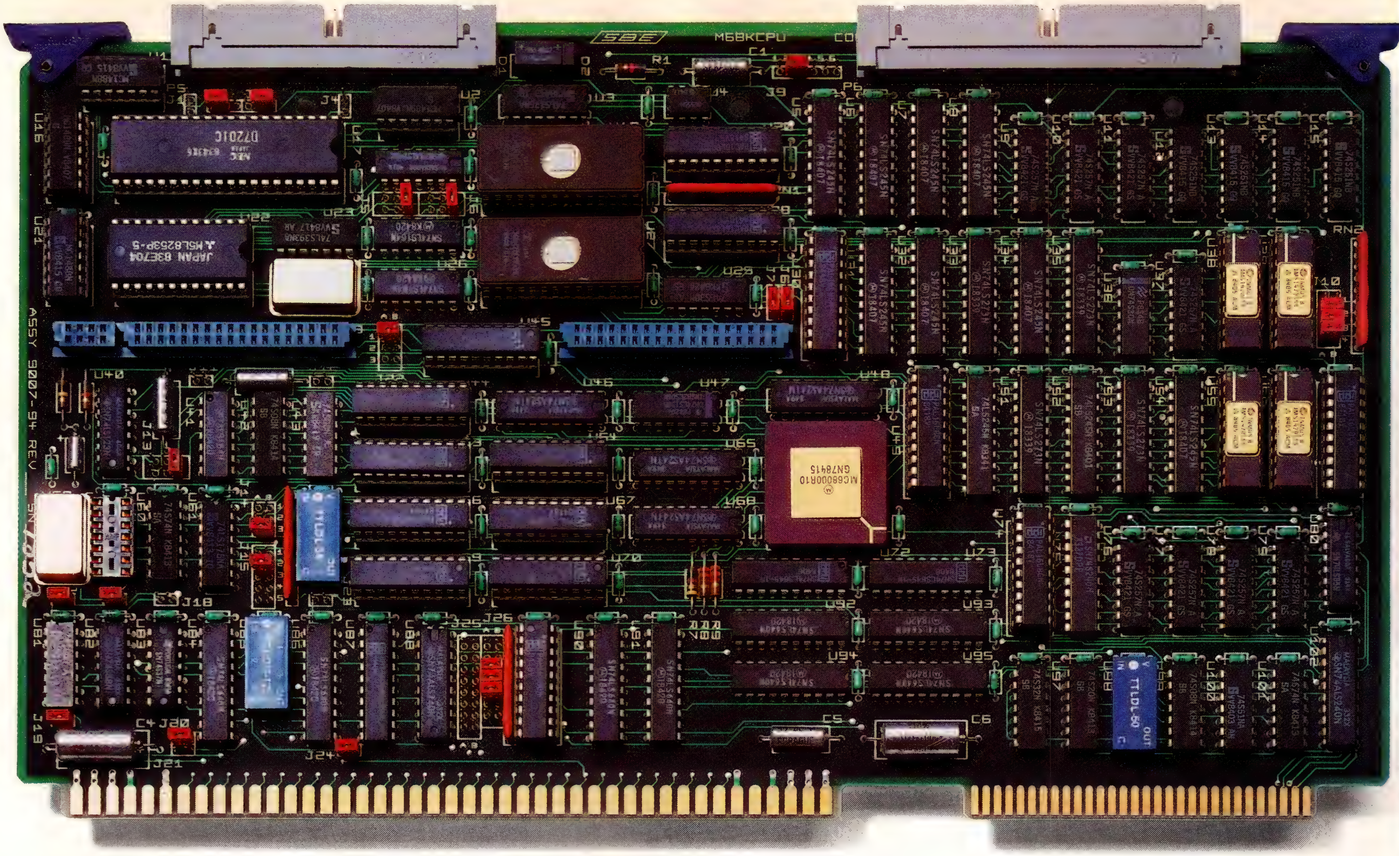
		HOST CHARACTERISTICS					
ERROR CORRECTION	FLAW SKIPPING	SUPPORT LEVEL	SIZE OF BUFFER (BYTES)	HOST TRANSFER RATE	MINIMUM INTERLEAVE	OEM PRICE (US)	COMMENTS
11-BIT BURST	SECTOR LEVEL	24-BIT ADDRESSING	ONE SECTOR	N/A	1:1	$2700	
11-BIT BURST	TRACK LEVEL	20-BIT ADDRESSING	ONE SECTOR	N/A	N/A	$2750	
N/A	N/A	ONBOARD iSBX EXPANSION	N/A	N/A	N/A	$1170	SINGE OR DOUBLE SIDED, SINGLE OR DOUBLE DENSITY
11-BIT BURST	N/A	20/24-BIT ADDRESSING	32k CACHE	N/A	N/A	$1450	iRMX/XENIX SUPPORT
11-BIT BURST	N/A	N/A	ONE SECTOR	N/A	N/A	$1650	MATES WITH iSBC 217/218, CONFIGURED AS iSBC 215 AND A DATA SEPARATOR BOARD
11-BIT BURST	N/A	N/A	ONE SECTOR	N/A	N/A	$2750	MATES WITH iSBC 217/218
N/A	N/A	NONE	NONE	N/A	N/A	$1795	ALSO HAS SCSI PORT AND ONBOARD CACHE, SINGLE OR DOUBLE DENSITY
11-BIT BURST	TRACK LEVEL	24-BIT ADDRESSING, DMA	NONE	N/A	SOFTWARE SELECTABLE	$1695	
11-BIT BURST	BAD-TRACK MAPPING	24-BIT ADDRESSING	ONE SECTOR	N/A	2:1	$2250	
8-BIT BURST	TRACK LEVEL	20-BIT ADDRESSING	NONE	N/A	N/A	$1995	
11-BIT BURST	TRACK LEVEL	24-BIT ADDRESSING	16k	3M-BPS DMA	1:1	$1695	UNIX OPTIMIZED, ONBOARD CACHE, IMAGE BACKUP
11-BIT BURST	TRACK AND SECTOR LEVEL	24-BIT ADDRESSING	16k	N/A	1:1	$2250	UNIX OPTIMIZED, ONBOARD CACHE
ECC (WIN-CHESTER)	N/A	24-BIT ADDRESSING	N/A	N/A	N/A	$795	
RETRY	SECTOR-LEVEL MAP	24-BIT ADDRESSING	N/A	N/A	1:1	$1035	
5-BIT BURST	SECTOR LEVEL	24-BIT ADDRESSING	N/A	N/A	1:1	$1035	
5-BIT BURST	SECTOR LEVEL	24-BIT ADDRESSING	N/A	N/A	1:1	$1165	
11-BIT BURST	N/A	24-BIT ADDRESSING	N/A	N/A	1:1	$1175	4 ARBITRATION MODES
11-BIT BURST	N/A	24-BIT ADDRESSING	N/A	N/A	1:1	$1345	

Table continued on pg 132

TABLE 2—MULTIBUS I MASS-STORAGE CONTROLLER CARDS *(continued)*

			DRIVE CHARACTERISTICS			
MANUFACTURER	MODEL NUMBER	CONTROLLER TYPE	DRIVE INTERFACE	MAXIMUM NUMBER OF DRIVES	SECTOR SIZES (BYTES)	ERROR DETECTION
QUALOGY	RAMTRAC 5317	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ESDI (WINCHESTER), SA450 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 TAPE	128 THROUGH 1k	32-BIT ECC
	RAMTRAC 6217B	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506 (WINCHESTER), SA850 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 TAPE	128 THROUGH 1k	32-BIT ECC
	RAMTRAC 7217B	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	SA1000 (WINCHESTER), SA850 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 TAPE	128 THROUGH 1k	32-BIT ECC
SCIENTIFIC MICRO SYSTEMS	FWD 8001	MULTIFUNCTION (WINCHESTER/ FLOPPY)	SA1000 (WINCHESTER), SA850 (FLOPPY)	2 WINCHESTERS, 2 FLOPPIES	128 THROUGH 1k	32-BIT ECC
	FWD 8006	MULTIFUNCTION (WINCHESTER/ FLOPPY)	ST506, SA850/450	2 WINCHESTERS, 2 FLOPPIES	128 THROUGH 1k	32-BIT ECC
	FWD 8007	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ST506 (WINCHESTER), SA850/450 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 TAPE	128 THROUGH 1k	32-BIT ECC
	FWD 8008	MULTIFUNCTION (WINCHESTER/ FLOPPY/TAPE)	ESDI (WINCHESTER), SA850/450 (FLOPPY), QIC-02 (TAPE)	2 WINCHESTERS, 2 FLOPPIES, 1 TAPE	128 THROUGH 1k	32-BIT ECC
WESPERCORP	MB-QIC-2	TAPE ONLY (¼-IN. CARTRIDGE)	QIC-02	4 TAPE DRIVES	512 BYTES	N/A (IN THE FORMATTER)
	MB-SMD	WINCHESTER ONLY (8- OR 14-IN.)	SMD (2.1M BYTES/SEC)	4 WINCHESTERS	PROGRAM-MABLE	32-BIT ECC
	MB506/1000	MULTIFUNCTION (WINCHESTER/FLOPPY)	SA1000/ST506 (WINCHESTER), SA450 (FLOPPY)	3 WINCHESTERS, 4 FLOPPIES	128 THROUGH 1k	32-BIT ECC
XYLOGICS	472	TAPE ONLY (9 TRACKS)	PERTEC	8 TAPE DRIVES	TO 2k	N/A (IN THE FORMATTER)
	450	WINCHESTER ONLY (8- OR 14-IN.)	SMD (1.9M BYTES/SEC)	4 WINCHESTERS	128 THROUGH 1k	32-BIT ECC
	421	MULTIFUNCTION (WINCHESTER/TAPE)	ST506 (WINCHESTER), QIC-02 (TAPE)	2 WINCHESTERS, 4 TAPES	256 THROUGH 1k	32-BIT CRC
	422	MULTIFUNCTION (WINCHESTER/TAPE)	ESDI (1.2M BYTES/SEC), QIC-02 (TAPE)	2 WINCHESTERS, 4 TAPES	256 THROUGH 1k	32-BIT ECC
	451	WINCHESTER ONLY (8- OR 14-IN.)	SMD (2.4M BYTES/SEC)	4 WINCHESTERS	256 THROUGH 1k	32-BIT ECC

		HOST CHARACTERISTICS					
ERROR CORRECTION	FLAW SKIPPING	SUPPORT LEVEL	SIZE OF BUFFER (BYTES)	HOST TRANSFER RATE	MINIMUM INTERLEAVE	OEM PRICE (US)	COMMENTS
11-BIT BURST	N/A	24-BIT ADDRESSING	N/A	N/A	1:1	$1375	
11-BIT BURST	N/A	24-BIT ADDRESSING	N/A	N/A	1:1	$1345	
11-BIT BURST	N/A	24-BIT ADDRESSING	N/A	N/A	1:1	$1345	
6-BIT BURST CORRECTION	TRACK LEVEL	16/20/24-BIT ADDRESSING	N/A	N/A	N/A	$1300	iSBC 215/iSBX 218 COMPATIBLE
6-BIT BURST CORRECTION	TRACK LEVEL	16/20/24-BIT ADDRESSING	N/A	N/A	N/A	$1200	iSBC 215 COMPATIBLE
6-BIT BURST	TRACK LEVEL	16/20/24-BIT ADDRESSING	N/A	N/A	N/A	$1000	iSBC 214 COMPATIBLE
6-BIT BURST	TRACK LEVEL	16/20/24-BIT ADDRESSING	ONE TRACK	N/A	N/A	$1200	iSBC 214 COMPATIBLE
N/A (IN THE FORMATTER)	BLOCK REWRITES	8/16-BIT DATA PATH	2k	N/A	N/A	$890	
11-BIT BURST	TRACK LEVEL	8/16-BIT DATA PATH	1.5k	N/A	PROGRAM-MABLE	$2100	iSBC 220 COMPATIBLE
11-BIT BURST	N/A	8/16-BIT DATA PATH	1k	N/A	PROGRAM-MABLE	$1060	
N/A (IN THE FORMATTER)	BLOCK REWRITES	16/20/24-BIT ADDRESSING	2k (8k OPTIONAL)	3M-BPS DMA	N/A	$1695	TRIDENSITY TAPE COUPLER TO 125-IPS SPEEDS
11-BIT BURST	SECTOR LEVEL	16/20/24-BIT ADDRESSING	2k (8k OPTIONAL)	3M-BPS DMA	1:1	$2295	
11-BIT-BURST	N/A	N/A	4k (DISK), 512 (TAPE)	2.5M-BPS DMA	1:1	$1695	
11-BIT BURST	SECTOR LEVEL	N/A	4k (DISK), 512 (TAPE)	2.5M-BPS DMA	1:1	$1795	
11-BIT BURST	SECTOR LEVEL	16/20/24-BIT ADDRESSING	2k (8k OPTIONAL)	3M-BPS DMA	1:1	$2495	



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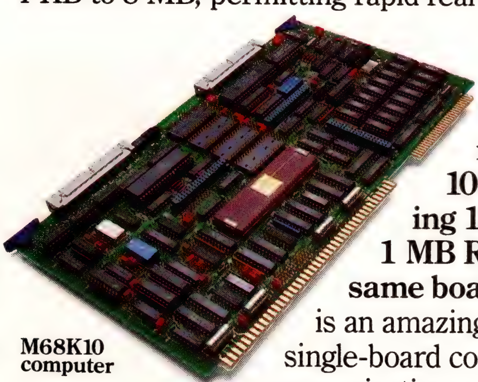

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CIRCLE NO 74

Basic programs solve differential equations quickly

Differential equations that describe the performance of various devices can be difficult to solve, but you can convert them to integral equations and let a small computer solve them with Basic-language programs.

Ron Rippy,
National Institute of Environmental Health Sciences

Obtaining analytical solutions to differential equations that describe devices such as electronic filters and shock absorbers can be difficult or even impossible. However, by using your computer's ability to run short, repetitive routines quickly, you can obtain very close approximations to most differential equations. To solve a differential equation, you first convert the equation into integral form and then let the computer sum the area under the equation's curve by rectangular integration **(Ref 1)**.

For example, a resistor and capacitor form a classic integrator circuit **(Fig 1)** whose performance can be described by a differential equation. The circuit produces a slowly increasing output voltage (E_0) after you connect the input voltage (V_0) to the circuit. A differential equation describes the circuit's transfer function, or the ratio between the two voltages:

$$\frac{E_0}{V_0} = \frac{1}{sRC + 1}. \qquad (1)$$

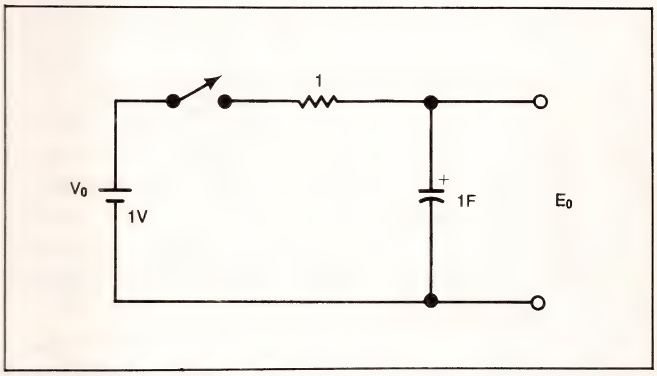


***Fig 1—A simple RC circuit** provides an example that lets you explore the use of Basic programs to solve differential equations.*

In **Eq 1,** s indicates a differential with respect to time. The term sE_0, for example, would represent dE_0/dt. Conversely, the notation 1/s represents an integral with respect to time, so E_0/s would represent $\int E_0 dt$.

The s terms let you quickly rearrange the equation and solve it for one unknown. Because you want to find out how the integrator's output voltage, E_0, changes after you close the switch, you rearrange **Eq 1** and solve it for the highest order differential term, sE_0. All the lower-order equation terms go on the right side:

$$sE_0 = -\frac{1}{RC} E_0 + \frac{1}{RC} V_0. \qquad (2)$$

To convert from a differential to an integral equation, divide each side of the equation by the highest order s term you find on the left side of the equation. In **Eq 2,** the highest order s term is simply s, so dividing each

Algorithms solve differential equations by applying numerical integration.

term on both sides of the equation by s yields

$$E_0 = -\frac{1}{RC}\frac{1}{s}E_0 + \frac{1}{RC}\frac{1}{s}V_0. \qquad (3)$$

Integral equations are relatively easy for a computer to solve because they involve repetitive addition operations that the computer does with software loops. To solve **Eq 3** and produce values of E_0 as it changes with respect to time, your program must include a statement like

E1=T*E0+E1

in a short DO or FOR-TO program loop. The program statement maintains a running sum (E1) of the output voltage. This running sum closely approximates the integral of the output voltage.

In effect, the program uses a rectangular-integration technique that finds the area under the E_0 vs t curve by breaking the curve into narrow rectangles. The program calculates the area of each rectangle in the T*E0 step and adds the area to the running total, E1. Keep in mind that rectangular integration doesn't give you an exact solution for an integral equation. To keep errors small, choose a short time interval (t, or T in the program code) for the integration program step so that the integrator circuit's output voltage E_0 won't change greatly during the interval.

Because **Eq 3** contains two 1/s, or integral, terms—one for E_0 and one for V_0—you must include two summation steps in your program:

E1=T*E0+E1
V1=T*V0+V1

By substituting E1 for E_0/s and V1 for V_0/s in **Eq 3,** you get the new output voltage from a third program line:

E0=−1/RC*E1+1/RC*V1

In other words, the integrator circuit's output voltage equals a constant (−1/RC) times the first integral of the output voltage, added to another constant (1/RC) times the first integral of the input voltage. The program in **Listing 1** solves the differential equation—now in integral form—and plots the results **(Fig 2)**. The computer plot shows the results you'll obtain for sample intervals (T) of 0.5 and 0.05 sec.

The result for the 0.5-sec integration period isn't accurate because the integrator circuit's output voltage, E_0, varies considerably during this period. When you specify 0.5-sec periods, however, the computer requires only seven passes through the program loop between lines 1040 and 1090. In complex programs you can use longer intervals to check your program and obtain rough results quickly.

Note that the program in **Listing 1** calculates the E1 value and uses it immediately to calculate E0. The V1 calculation, however, takes place later in the loop, and its value isn't used until the computer makes its next pass through the loop. By calculating V1 later in the loop, you ensure that the voltage across the capacitor is 0V at the start of the program, a practice learned from experience.

When the sample intervals are small, you can have the computer calculate V1 before it calculates E0. When you use large sample intervals, however, the order is important. For example, if you choose an

LISTING 1

```
1000 E0,E1,V1=0 @ V0,R,C=1
1010 SCALE 0,3,0,1
1020 XAXIS 0, .5 @ YAXIS 0, .25
1030 MOVE 0,0 @ T=.5
1040 FOR X=0 TO 3 STEP T
1050 E1=T*E0+E1
1060 E0=-(1/R*C*E1)+1/R*C*V1
1070 V1=T*V0+V1
1080 DRAW X,E0
1090 NEXT X
1100 END
```

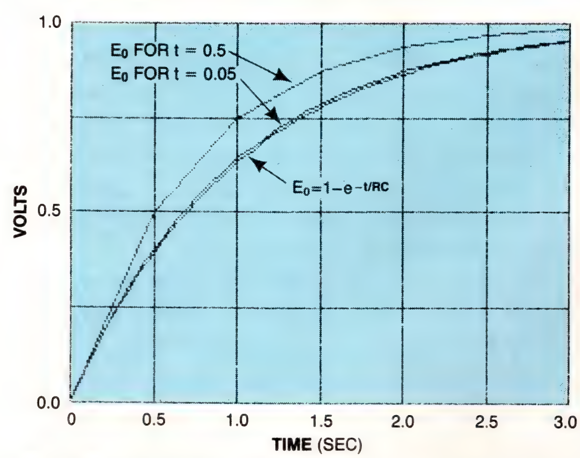


Fig 2—A plot of E_0 vs t for an RC circuit *illustrates that sample-interval selection influences the output-voltage calculation. Long sample intervals provide poor approximations for the rectangular-integration method.*

interval of 0.5 sec and program the computer to calculate V1 before it calculates E0, the computer plots a 0.5V output from the circuit as soon as you close the switch—a condition you know can't exist.

By reducing the sample interval to 0.05 sec, you improve the accuracy of the numerical integration because E_0 changes only slightly during each integration period. When you use a 0.05-sec period, the calculated result closely approximates the differential equation's exact mathematical solution, $E_0=1-e^{-t/RC}$. After one second, the accuracy of the results for sample intervals of 0.5, 0.05, and 0.005 sec is 18.6%, 1.49%, and 0.146%, respectively.

Solve multiple integrations

The RC integrator circuit requires only a single integration of variables. Equations that require two integrations are slightly more complex. Consider an RLC filter circuit **(Fig 3)** that requires a second-order differential equation to describe its transfer function:

$$\frac{E_0}{V_0} = \frac{1}{LCs^2 + \frac{L}{R}s + 1}. \qquad (4)$$

The equation calculates the ratio of the input and output voltages after you close the switch and apply voltage to the circuit. With ω standing for the filter's natural frequency (W in the program code), use the relationships $\omega=1/\sqrt{LC}$ and $Q=\omega \cdot R \cdot C$ to simplify **Eq 4** and put the highest order derivative term, s^2E_0, on the left:

$$s^2 E_0 = -\frac{\omega}{Q} sE_0 - \omega^2 E_0 + \omega^2 V_0.$$

Then divide each side of the equation by s^2 to yield

$$E_0 = -\frac{\omega}{Q}\frac{1}{s} E_0 - \omega^2 \frac{1}{s^2} E_0 + \omega^2 \frac{1}{s^2} V_0. \qquad (6)$$

Now the original second-order differential equation is in integral form, and you can use your computer to solve it. You must, however, calculate both the first and second integral of E_0. Calculate the first integral of E_0 the same way you calculated it in the program for the RC integrator circuit and then integrate the result to give the second integral of E0:

E1=T*E0+E1
E2=T*E1+E2

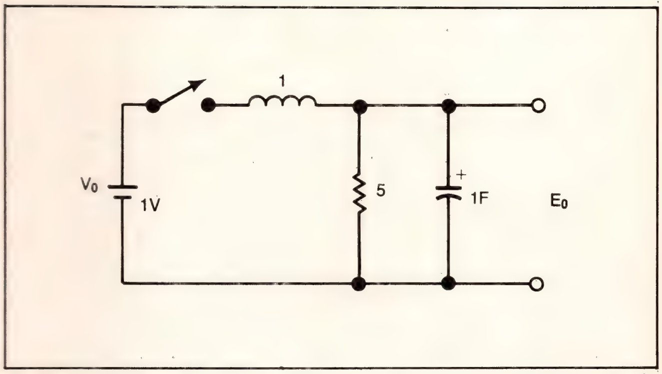


*Fig 3—**A typical RLC filter circuit** provides an example of a circuit that requires two integration steps to calculate its output voltage.*

Calculate the second integral of V_0 the same way:

V1=T*V0+V1
V2=T*V1+V2

Once you calculate E1, E2, and V2, substitute those values into **Eq 6** and calculate E_0. Your computer program requires an equivalent summation step to calculate E0:

E0 = −W/Q*E1−W*W*E2+W*W*V2

You can calculate the second integral of V_0 before or after the summing equation, but placing the calculation after the equation assures you that the program starts with a value of 0V across the output capacitor. The complete Basic program **(Listing 2)** includes the calculations for E1, E2, V1, V2, and E0. When you run the program, the computer calculates and plots a damped sine wave **(Fig 4)** as the filter circuit's output.

When you close the switch, the RLC filter circuit

LISTING 2

```
2000 EØ,E1,E2,V1,V2=Ø @ VØ=1
2010 W=1 @ Q=5
2020 SCALE Ø,7*PI,Ø,2
2030 XAXIS 1,PI/2 @ YAXIS Ø,.5
2040 MOVE Ø,Ø @ T=.Ø5
2050 FOR X=Ø TO 7*PI STEP T
2060 E1=T*EØ+E1
2070 E2=T*E1+E2
2080 EØ=-(W/Q*E1)-W*W*E2+W*W*V2
2090 V1=T*VØ+V1
2100 V2=T*V1+V2
2110 DRAW X,EØ
2120 NEXT X
2130 END
```

Use your computer's ability to run repetitive routines that closely approximate most differential equations.

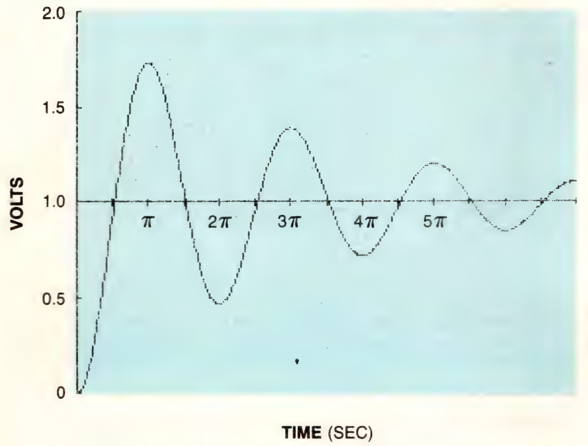


Fig 4—A damped sine wave or ringing signal *results when you run the program in* ***Listing 2.***

responds to the 1V signal by generating a damped sine wave or ringing signal with a 1-radian/sec frequency. You can test the circuit's response to other input voltages by substituting different values for V0 in the program. Instead of using a fixed voltage for V0 in the program, you can include an equation that calculates V0 voltages that vary with time.

As a final example of the integration technique, consider a tracking filter circuit **(Fig 5)** that locks onto an input signal and tracks changes in frequency, as long as they aren't too great and don't take place too quickly. Tracking filters correct Doppler shifts that arise in signals from communication satellites.

The filter tracks and cancels the slowly changing Doppler shifts caused by the satellite's orbital motion. The network passes high-frequency data-communication signals because the lowpass filter prevents them from generating a correcting feedback voltage. However, the filter passes low-frequency signals and generates a feedback voltage that corrects the input signal. The feedback circuit is a third-order lowpass filter.

The tracking filter's transfer function is expressed in the following equation:

$$\frac{E_0}{V_0} = \frac{s^3}{s^3 + 2\omega s^2 + 2\omega^2 s + \omega^3}.$$

To solve the filter's transfer function, first rearrange it so that it expresses E_0 as the highest order differential

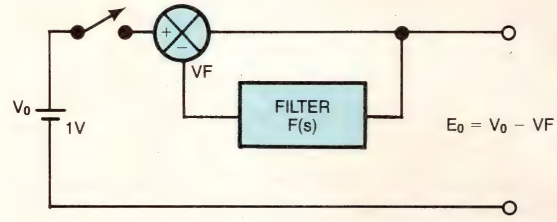


Fig 5—A third-order tracking filter *generates a feedback voltage that cancels slow variations in the input signal. The circuit is useful in tracking communication-satellite signals that are subject to the Doppler effect.*

on the left side of the equation:

$$s^3E_0 = -2\omega s^2E_0 - 2\omega^2 sE_0 - \omega^3E_0 + s^3 V_0.$$

Next, divide each side of the equation by s^3 to solve for E_0, and transform the equation into integral form:

$$E_0 = -2\omega \frac{1}{s} E_0 - 2\omega^2 \frac{1}{s^2} E_0 - \omega^3 \frac{1}{s^3} E_0 + V_0. \quad \mathbf{(9)}$$

To solve **Eq 9** and compute values of E_0, you must write a program that calculates the first, second, and third integrals of E_0.

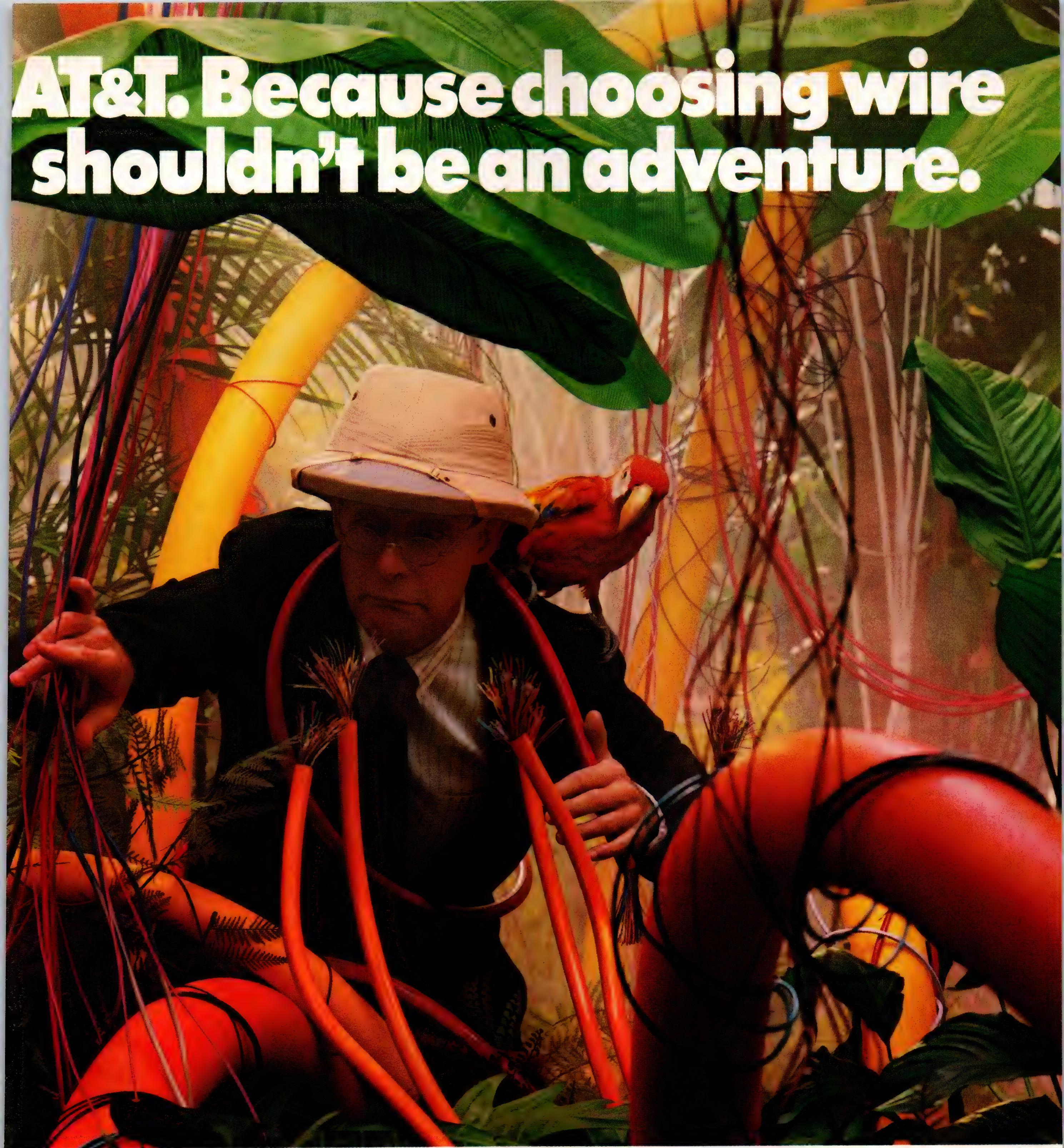
```
E1=T*E0+E1
E2=T*E1+E2
E3=T*E2+E3
E0=-2*W*E1-2*W*W*E2-W*W*W*E3+V0
```

The complete program **(Listing 3)** presets the filter's natural frequency (W) to 1 radian/sec.

When you close the switch, you create an error signal

LISTING 3

```
3000 E0,E1,E2,E3=0 @ V0,W=1
3010 SCALE 0,8,-.5,1.5
3020 XAXIS 0,1 @ YAXIS 0,.1
3030 MOVE 0,0 @ T=.05
3040 FOR X=0 TO 8 STEP T
3050 E1=T*E0+E1
3060 E2=T*E1+E2
3070 E3=T*E2+E3
3080 E0=-(2*W*E1)-2*W*W*E2-W*W*W*E3+V0
3090 DRAW X,E0
3100 NEXT X
3110 END
```



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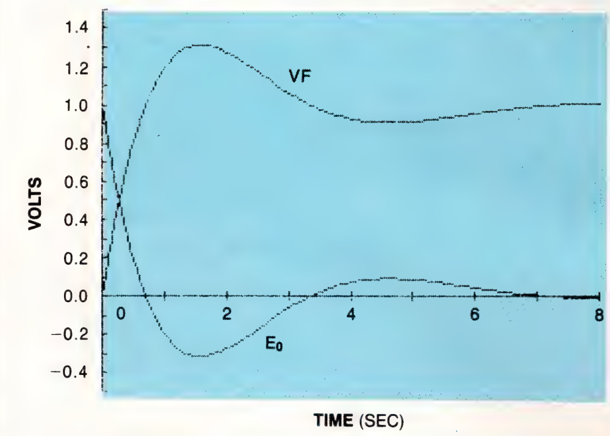
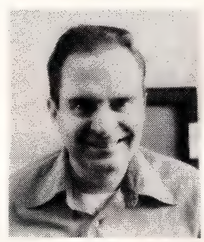


Fig 6—A plot of output and feedback voltages for a tracking filter *illustrates how a short computer program* ***(Listing 3)*** *simulates complex filter behavior.*

of 1V, or an input-signal phase error of 1 radian. The filter counteracts the 1V error by applying an equal and opposite voltage (VF) to the input signal. The filter can't act instantaneously, however, and it must conform to the time constraints of the filter circuit. Consequently, at first E_0 equals V_0, and the filter's feedback voltage is 0V. The feedback voltage increases, however, and eventually cancels the error voltage **(Fig 6),** thereby tracking the error voltage. **EDN**

Author's biography



Ron Rippy is an electronic engineer with the Laboratory of Molecular Biophysics at the National Institute of Environmental Health Sciences in Research Triangle Park, NC. Ron designs and maintains nuclear magnetic resonance (NMR) spectrometers and has 22 years of experience in designing RF circuits and in programming computers. He enjoys programming a VAX computer at work and includes reading among his leisure activities.

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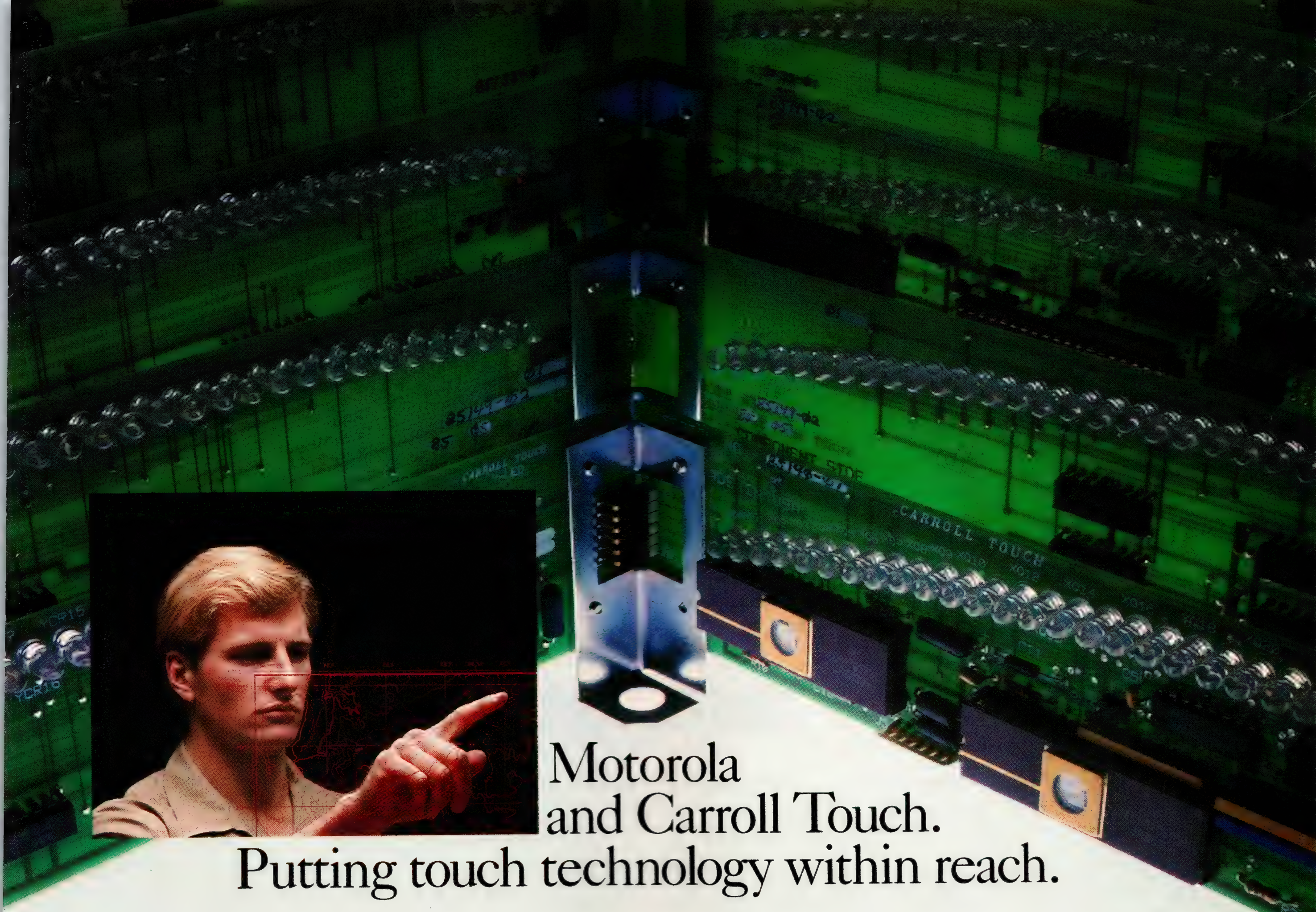

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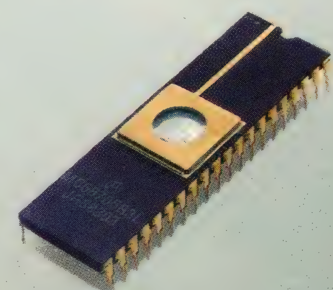

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Floating-point μP implements high-speed math functions

This final article in a 3-part series describes how to incorporate a floating-point processor into your system. It discusses criteria for the selection of the algorithms you'll use, and in particular it details the methods used to implement transcendental functions.

David Quong, *Advanced Micro Devices*

If your application must perform a variety of math functions at high speeds on a wide range of input data, consider designing a math subsystem based upon a VLSI floating-point processor. A floating-point processor, a microsequencer, RAM, and ROM, configured as shown in **Fig 1,** together with the appropriate algorithms, will allow you to perform most math functions at real-time speeds with high precision and a very large dynamic range. A system of this type will outperform even the fastest floating-point coprocessor.

The choice of algorithms is an important step in the realization of your math processor. You can choose from a variety of methods for implementing transcendental and other math functions: The Taylor series, the Chebyshev series expansion, and the Newton-Raphson approximation are just a few of the many possible approaches. Which algorithm is the best one for your particular application will depend upon what functions you want to perform, the hardware architecture you are using, and the system throughput and accuracy you expect to receive.

Many designers select the Taylor series for performing math functions. This well-known method allows you to find equations for various functions in most books of math tables. The Taylor series has a major drawback, however: It has a nonuniform convergence rate in the number of terms needed to achieve a desired accuracy. Consider, for example, the Taylor series expansion of the sine function:

$$\sin(x) = x - \frac{x^3}{3!} + \frac{x^5}{5!} - \frac{x^7}{7!} \cdots$$

For values of x near zero radians, this equation converges very quickly, but as x becomes larger, you'll need a larger number of terms to evaluate sin(x) to the same accuracy that you obtained for the smaller values.

The Chebyshev expansion method, like the Taylor method, produces a polynomial approximation, but it's not so well known. The generation of the Chebyshev approximation for a particular function is more complex than for the Taylor series, but the resulting polynomial is just as easy to implement. The major advantage of the Chebyshev method is that it has uniform convergence. Moreover, for any given function, over the operating range of the Chebyshev series this method yields smaller errors than almost any other method. You can usually determine by inspection the upper bound of the error; the error of the truncated series

A math-processing subsystem incorporating a VLSI floating-point processor will outperform even the fastest available floating-point coprocessor.

cannot exceed the sum of the absolute values of the remaining Chebyshev coefficients. (For details of the derivation of the Chebyshev series, see **box,** "Deriving a Chebyshev series.")

Iteration handles simple functions

For some simple functions such as division and square-root extraction, the Newton-Raphson method, an iterative approach for approximating such functions, works well. When using this or any other iterative method, you have to start with a seed, or initial approximation. The better this approximation is, the faster will be the convergence. You can store predetermined seed values in a look-up table. This method usually requires extra hardware (in the form of ROMs), but it gives you flexibility, because you can store seed values that are as accurate as you want.

The chief attraction of the Newton-Raphson method is its rapid convergence; the number of iterations required is low. The method converges quadratically, ie, the order of the error is squared by each iteration. For example, if the seed is accurate to eight bits, the first iteration improves the accuracy to 16 bits, and the second iteration improves it to approximately 32 bits (variance depends on the magnitude of the error).

The math processor shown in **Fig 1** evaluates Chebyshev and Newton-Raphson approximations very efficiently. The system performs transcendental (trigonometric, logarithmic, and exponential) functions by the Chebyshev method and division and square-root extraction by the Newton-Raphson method.

Understand the algorithms

The algorithms for 10 very common math functions are described below. You'll need these functions for applications associated with navigation, guidance, image processing, signal processing, and many other areas. The algorithms for the transcendental functions are based on the Chebyshev method and consist of a 3-stage process. The first stage reduces the range of

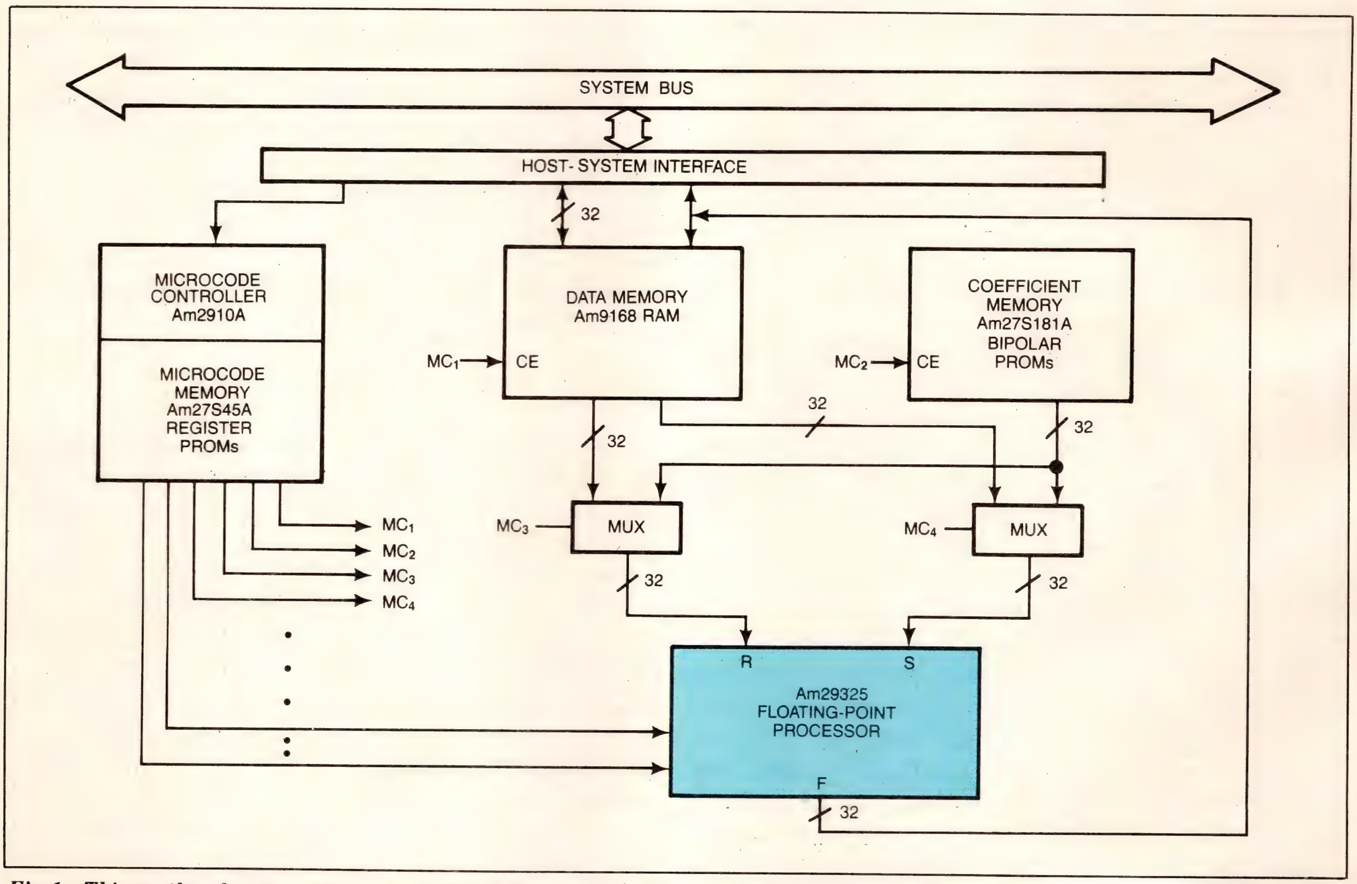

***Fig 1—This math subsystem** is based on a VLSI floating-point processor. It performs math functions with high precision and a large dynamic range.*

Deriving a Chebyshev series

The Chebyshev series expansion is a procedure for generating a polynomial approximation for a given math function, f(x). To expand the function, you must express it as a Chebyshev series:

$$f(x)=0.5C_0+C_1T_1(x)+C_2T_2(x)+\ldots$$

for $-1\le x\le 1$, where $T_n(x)$ is the Chebyshev polynomial of degree n given by

$$T_n(x)=\cos(n\times \operatorname{acos}(x))$$

and C_n is a coefficient of the Chebyshev series. The value of C_n is dependent upon the function f(x). You can determine the value of C_n by evaluating the following relationship:

$$C_n=\frac{2}{\pi}\int_{-1}^{+1}\frac{f(x)\,T_n(x)}{\sqrt{1-x^2}}\,\delta x.$$

Alternatively, you can obtain the C_n coefficients in tabular form, for a wide variety of functions, from books on mathematical tables **(Ref 2).**

Examples of the $T_n(x)$ polynomial include the following:

$$\begin{aligned}T_0(x) &= \cos(0) = 1\\ T_1(x) &= \cos(\operatorname{acos}(x)) = x\\ T_2(x) &= \cos(2\operatorname{acos}(x))\\ &= 2\cos^2(\operatorname{acos}(x))\\ &= 2x^2-1.\end{aligned}$$

You can generate a polynomial equation for a function by combining the above equations and combining terms with common exponents. The accuracy of the result depends upon the number of terms you use. (If you are interested in a formal derivation of the Chebyshev method, see **Refs 1** and **2**.)

Expansion for sine function

If you want to find the Chebyshev expansion for the sine function, first go to the coefficient tables in **Ref 2** and look up the coefficients for the sine function (or calculate them from the formula given above). Next, determine the number of coefficients required to provide the accuracy you want. For example, to achieve 24 bits of accuracy, the error should be no greater than one part in 17 million. Compare the magnitude of this largest acceptable error with each of the coefficients. The first term that contains a coefficient that's less than the error can be the last term in the series. It's common practice, however, to include one extra term in the series.

Using the above criteria, you need only six coefficients for the sine function using $\sin(\frac{1}{2}\pi x)$ in order to obtain a result that's accurate to 24 bits. These coefficients are

- $C_0=C_{sin0}=+2.552557925$
- $C_1=C_{sin1}=-0.285261569$
- $C_2=C_{sin2}=+9.118016007\times10^{-03}$
- $C_3=C_{sin3}=-1.365875135\times10^{-04}$
- $C_4=C_{sin4}=+1.184961858\times10^{-06}$
- $C_5=C_{sin5}=-6.702792\times10^{-09}$

Substituting the T_nx polynomials into the Chebyshev series gives

$$\begin{aligned}\sin(\tfrac{1}{2}\pi x) =\;& 0.5C_0 + C_1x + C_2(2x^2-1)\\ &+ C_3(4x^3-3x)\\ &+ C_4(8x^4-8x^2+1)\\ &+ C_5(16x^5-20x^3+5x).\end{aligned}$$

Simplifying the terms gives

$$\sin(\tfrac{1}{2}\pi x) = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5.$$

where

- $a_0=(0.5)C_0-C_2+C_4$
- $a_1=C_1-3C_3+5C_5$
- $a_2=2C_2-8C_4$
- $a_3=4C_3-20C_5$
- $a_4=8C_4$
- $a_5=16C_5$.

The final result for the sine function is a simple polynomial equation that you'll find easy to implement. You can precalculate the coefficients a_0 through a_5 and store them in a ROM table. You can apply the same procedure to any well-behaved function for which you can find or compute the Chebyshev coefficients.

The Chebyshev expansion method, like the Taylor method, produces a polynomial approximation, but it's not so well known.

the input arguments to values between +1 and −1, because the Chebyshev expansion operates only over this range. The second stage evaluates the polynomial derived from the Chebyshev expansion. The third stage performs any postprocessing that may be required, such as correction of the sign.

The detailed descriptions were developed by Clenshaw, Miller, and Woodger (**Ref 1**). They use the terms RND and CSERIES: RND indicates that the result of the operation must be rounded towards minus infinity, and CSERIES indicates that the Chebyshev series for the input must be evaluated.

Range reduction prepares arguments

The range-reduction steps for the sine function are

- $x=x(2/\pi)$
- $x=x-(4(RND(0.25(x+1))))$
- If $x>1$ then $x=2-x$.

As noted, these steps reduce the input argument to the range $-1 \le x \le 1$. You then evaluate the sine function by summing the terms of the following polynomial equation derived for the sine function:

$$\sin(x)=x(CSERIES_{sin}(2x^2-1)).$$

The range-reduction steps for the cosine function are

- $x=x(2/\pi)$
- $x=4(RND(0.25(x+2)))-x+1$
- If $x>1$ then $x=2-x$.

You then evaluate the cosine function by using the same polynomial equation as for the sine function:

$$\cos(x)=x(CSERIES_{sin}(2x^2-1)).$$

The range-reduction steps for the tangent function are

- $x=x(2/\pi)$
- $x=x-(4(RND(0.25(x+1))))$
- $y=x$
- If $x>1$ then $x=2-x$.

The Chebyshev polynomial evaluation for the tangent function is

$$\tan(x)=x(CSERIES_{tan}(2x^2-1)).$$

You have to perform one postprocessing step:

$$\text{If } y>1 \text{ then } \tan(x)=1/\tan(x).$$

You don't need any range-reduction steps for the arcsine function, because all values outside the range $-1 \le x \le 1$ indicate an error condition. For input arguments in the range $x^2 \le \frac{1}{2}$, you evaluate the arcsine as follows:

$$\text{asin}(x)=x(\sqrt{2}(CSERIES_{asin}(4x^2-1))).$$

For input arguments in the range $\frac{1}{2}<x^2 \le 1$, you evaluate the arcsine as follows:

$$\text{asin}(x)=\text{sign}(x)(\pi/2)(\sqrt{2-2x^2})(CSERIES_{asin}(3-4x^2)),$$

where sign(x) is the sign of x.

You use the following trigonometric identity to evaluate the arc-cosine function:

$$\text{acos}(x)=\pi/2-\text{asin}(x).$$

The range-reduction steps for the arctangent function are

- $u=x$
- If $ABS(x)>1$ then $x=1/x$,

where ABS(x) is the absolute value of x. The Chebyshev polynomial evaluation is

$$\text{atan}(x)=x(CSERIES_{atan}(2x^2-1)).$$

The postprocessing steps are

$$\text{If } u>1 \text{ then atan}(x)=+(\pi/2)-\text{atan}(x)$$

and

$$\text{If } u<-1 \text{ then atan}(x)=-(\pi/2)-\text{atan}(x).$$

The range-reduction steps for the exponentiation function are

- $x=x(\log_2 e)$
- $N=1+RND(x)$.

The Chebyshev polynomial evaluation is

$$\exp(x)=2^N(CSERIES_{exp}(2(N-x)-1)).$$

Only positive values are valid input arguments for the natural-log function; a zero or a negative value should be flagged as an error:

$$\ln(x)=(CSERIES_{ln}(4(\text{mant}(x))-3))+(\text{expo}(x)-1)(\ln(2)),$$

where mant(x) is the mantissa value of x, expo(x) is the exponent value of x, and ln(2) is a constant value.

You perform division operations by evaluating the

reciprocal function. For example, you can express the division operation C=A/B in its reciprocal form, C=A(1/B). By using the Newton-Raphson method, you can find an iterative expression for the reciprocal function. This expression is

$$x_{i+1}=x_i(2-B(x_i)),$$

where x_0 is the initial divisor reciprocal (seed value) for i=0, and X_i is the *ith* approximation.

The square-root function also uses the Newton-Raphson method. The iterative expression for the inverse square-root function is

$$x_{i+1}=0.5(x_i(3.0-Ax_i^2)).$$

You then evaluate the square root of A by the equation

$$B=A(x_{i+1}),$$

where A is the input argument, B is the square root of A, x_0 is the initial approximation (seed value) for i=0, and x_i is the *ith* approximation.

The principal component of the math-processor subsystem described here is the Am29325 floating-point processor. The subsystem also contains RAM, bipolar PROMs to store coefficients, a subsystem controller, and a host interface. The floating-point processor performs all computations under control of the subsystem controller; microcoded programs to perform the functions you need reside in the subsystem controller's PROM. If you wish to modify existing functions or add new functions, you merely change the microprogrammed PROM.

The Am29325 floating-point processor **(Fig 2)** provides many features that simplify subsystem design. The 3-port, 32-bit I/O structure of the Am29325 avoids data multiplexing and allows efficient transfer of information. The 32-bit internal registers and data paths allow the chip to store the results of intermediate calculations for use in subsequent operations, thereby avoiding the delays that transfer of these results to and from off-chip storage would entail. Many functions don't need to send data out of the chip until the final results of an operation are ready.

The floating-point-processor hardware detects exceptional conditions and, rather than compounding the error until the end of the calculation, immediately notifies the host system. The chip notifies the host by means of flags that indicate underflow, overflow, invalid operation, and other error conditions.

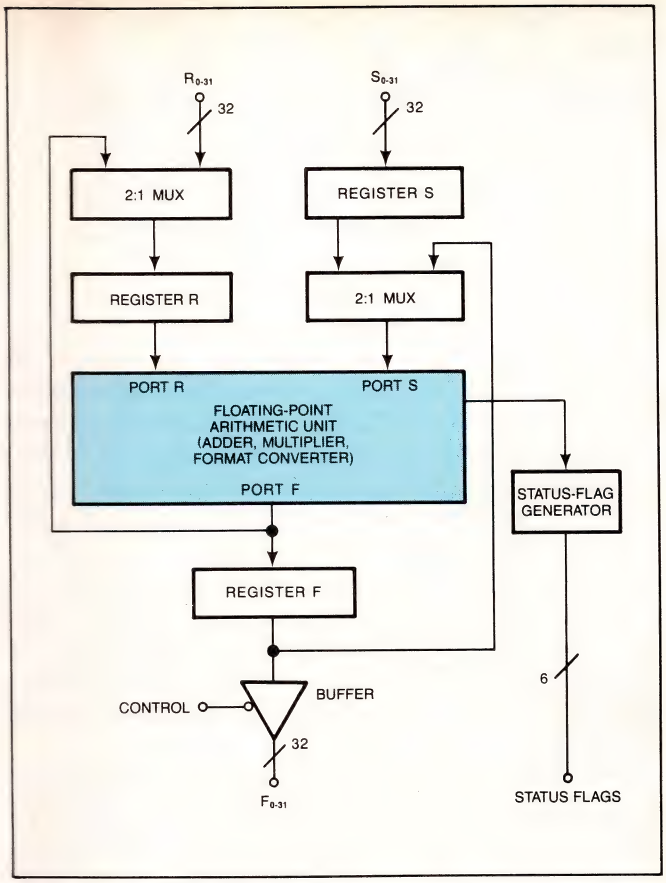

Fig 2—This VLSI floating-point processor is fast *because it contains all the major components for 32-bit operations on a single chip. It has one input for an external clock and 17 inputs for instruction-select and control functions.*

Subsystem data storage consists of a high-speed, 4-port RAM. You can load the data memory from the host computer (using DMA), from the floating-point processor, or from an integer processor. You'll need to process integers during operations such as isolating the exponent and mantissa portions of a floating-point word. You can have the host processor perform integer processing, or you can arrange it so that the math subsystem performs the required operations by incorporating an integer processor chip in your design.

Learn to microprogram the processor

Two examples of how to implement math functions on the Am29325 floating-point processor will give you an introduction to the microcoding procedures you'll use in the math processor. Recall, that, for a given division operation (C=A/B), the Newton-Raphson division algorithm begins by obtaining the reciprocal of the divisor by means of an iterative equation. A single iteration requires just three arithmetic operations:

- multiplication: $B(x_i)=u$
- subtraction: $2-u=v$
- multiplication: $v(x_i)=x_{i+1}$.

You can microcode this procedure with a 3-instruction loop that you repeat until you obtain a sufficiently accurate value of x_{i+1}. You then perform a single multi-

The math processor uses the Newton-Raphson method to execute the division and square-root functions.

plication, $A \times x_{i+1}$, to obtain the quotient.

The conventional way to obtain a seed is to use the most significant 16 or so bits of the divisor as a pointer into a look-up table in ROM; the contents of the address to which the divisor bits point become the seed output, which usually has approximately the same number of bits. You might think that use of a 16-bit address would require a ROM that's 64k words deep, but this is not so. In floating-point division, you can reciprocate the exponent and significand separately, each from its own table, and then recombine them. Consequently, for an 8-bit exponent and the eight most significant bits of the significand, you require only two tables, each just 256 words deep.

You can also trade ROM word width for execution time (ie, the number of iterations); doubling the width of the significand stored in ROM will reduce reciprocal refinement time by roughly one iteration. Convergence is specified by the inequality $2/B > |x_0| > 0$.

The microcoding for the complete Newton-Raphson division is shown in **Table 1.** The operation requires six lines of microcode. In cycle 1, you load the seed into register R of the floating-point processor and load the divisor into register S. In cycle 2, you multiply the contents of registers R and S; the result appears in register F.

In cycle 3, you perform the subtraction, using the 2−S instruction of the floating-point processor. The input for port S comes from register F via the internal feedback path. The result of the subtraction appears in register F.

In cycle 4, you perform the second multiplication. This operation multiplies the contents of register F (via port S) by x_i (from register R). The result, x_{i+1}, replaces x_i in register R. In parallel with the multiplication, the microsequencer executes a jump back to cycle 2 to begin the next iteration.

Cycle 5 begins after the last iteration of cycles 2 through 4. In this cycle, you load the dividend (A) into register S and multiply it by the contents of register R to produce the final result. This result appears in register F, from which you can unload it via the F bus to local data storage or to the host.

The second implementation example uses the Chebyshev method to perform a sine calculation. In the polynomial equation that evaluates the sine function,

$$\text{CSERIES}_{\sin} = a_0 + a_1x + a_2x^2 + a_3x^3 + a_4x^4 + a_5x^5.$$

The range-reduction steps require eight or nine operations. Evaluation of the polynomial equation requires 23 additional operations, including processing of the $2x^2-1$ expression. One final operation multiplies the result of the polynomial evaluation by x. The sine function therefore requires 32 or 33 operations.

You can, however, save 10 cycles in the evaluation of

TABLE 1—INSTRUCTION SEQUENCE FOR NEWTON-RAPHSON DIVISION ON THE Am29325

CLOCK CYCLE	I0-ALU SELECT	I1-ALU SELECT	I2-ALU SELECT	I3-SMUX CONTROL	I4-RMUX CONTROL	$\overline{\text{ENR}}$-R REG ENABLE	$\overline{\text{ENS}}$-S REG ENABLE	$\overline{\text{ENF}}$-F REG ENABLE	$\overline{\text{OE}}$-OUTPUT ENABLE	ALU OPERATION	CONTENT OF REG R	CONTENT OF REG S	CONTENT OF REG F	COMMENT
1	X	X	X	X	0	0	0	X	X	X	?	?	?	LOAD B AND SEED INTO Am29325
2	0	1	0	0	X	1	1	0	X	R*S	X(0)	B	?	BEGIN FIRST ITERATION
3	1	1	0	1	X	1	1	0	X	2−S	X(0)	B	B*X(0)	
4	0	1	0	1	1	0	0	0	X	R*S	X(0)	B	2−B*X(0)	X(1)=X(0)[2−B*X(0)], LOAD A
5	0	1	0	0	X	1	1	0	X	R*S	X(1)	A	X(1)	A*X(1), X(1)=1/B
6	X	X	X	X	X	X	X	X	0	X	X(1)	A	A*X(1)	OUTPUT RESULT, A/B

X=DON'T CARE ?=UNKNOWN

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The floating-point processor hardware detects exceptional conditions and, rather than compounding the error, immediately notifies the host system.

the polynomial equation by applying Horner's Rule, an algebraic method for rearranging components in a polynomial. The polynomial equation then becomes

$$\text{CSERIES}_{\sin}=((((a_5x+a_4)x+a_3)x+a_2)x+a_1)x+a_0.$$

The total number of operations in the sine function then decreases to 22 or 23. Evaluation of the rearranged polynomial equation is complete in 10 clock cycles.

In cycle 1, you load x into the S register and a_5 into the R register. Multiply these two operands to produce $a_5 \times x$. In cycle 2, you load the result of the multiplication into the F register, load a_4 into the R register, and add the contents of the F and R registers to yield

$$(a_5 \times x)+a_4.$$

In cycle 3, you load the result of the addition into the R register; the S register still contains x. Perform $R \times S$ to obtain

$$((a_5 \times x)+a_4)x.$$

Cycles 4 through 10 perform similar addition and multiplication operations, progressively using the terms a_3 through a_0. The final result of evaluating the polynomial equation is available in the F register after cycle 10.

The ability to perform both simple and complex math functions rapidly is critical in systems that process data in real time. You won't yet find many simple, compact solutions to this problem on the market. Math-coprocessor ICs are available, but they are still in the low- to medium-performance range, and they limit you to a microprocessor environment. (**Table 2** shows comparative timings for two floating-point coprocessor chips and the Am29325 floating-point processor.)

You can design and build your own MSI chip, but such a product will require much development time and cost, and it will probably be large and consume lots of power. Another possible approach is to compute the values of the math functions you will need and to store these values in ROM, but such a look-up-table method is adequate only for small amounts of data. At the present time, the use of a math subsystem based upon a VLSI floating-point processor with a relatively small amount of support circuitry appears to be the most cost-effective solution. **EDN**

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1. Clenshaw, CW, Miller, GF, and Woodger, M, "Algorithms for Special Functions I," *Numerische Mathematik*, Vol 4, 1963, pg 403. See also Miller, GF, "Algorithms for Special Functions II," *Numerische Mathematik*, Vol 7, 1965, pg 194.
2. Clenshaw, C W, "Chebyshev series for mathematical functions," Vol 5 of the Mathematical Tables of the National Physical Laboratory, HM Stationery Office, London, 1962.

Author's biography

David Quong is an engineer in the product planning division of Advanced Micro Devices (Sunnyvale, CA). He received a BSEE from California State University at Sacramento, and in his spare time enjoys fishing, hiking, and skiing.

TABLE 2—TIMING COMPARISON OF SINGLE-PRECISION FLOATING-POINT FUNCTIONS

FLOATING-POINT CHIP	SPEED (MHz)	ADD (μSEC)	MULTIPLY (μSEC)	DIVISION (μSEC)	SQUARE ROOT (μSEC)	SINE (μSEC)	COSINE (μSEC)	TANGENT (μSEC)
INTEL 8087[1]	8.0	12.5	18.1	25.4	23.3	NOTE 3	NOTE 3	67.5
MOTOROLA 68881[2]	16.67	2.8	3.1	3.8	N/A	23.0	23.0	27.2
AMD Am29325	8.0	0.125	0.125	1.125	1.625	2.875	3.125	4.750

NOTES:

N/A = TIMES NOT AVAILABLE.

1. TIMES FOR THE INTEL 8087 WERE DERIVED FROM THE INSTRUCTION CLOCK COUNT GIVEN IN THE INTEL DATA PAMPHLET (1984). ALL TIMES LISTED ARE WORST CASE.
2. TIMES FOR THE MOTOROLA MC68881 WERE TAKEN FROM A NEWS ITEM IN *ELECTRONIC PRODUCTS*, FEBRUARY 15, 1985, PG 43.
3. THIS OPERATION IS NOT COVERED BY THE INSTRUCTION SET AND MUST BE IMPLEMENTED BY USING OTHER INSTRUCTIONS.

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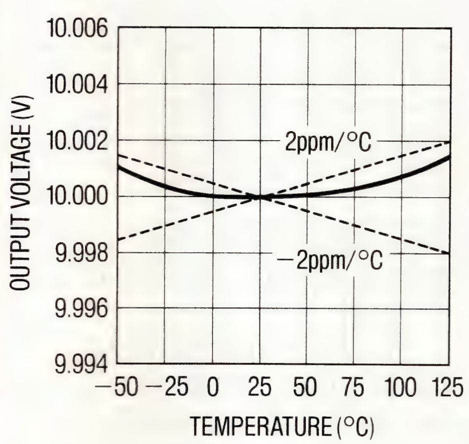

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CIRCLE NO 80

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Use simple circuit to program EPROMs

Richard Poindexter
Telex Computer Products, Tulsa, OK

You can program 21V, 28-pin EPROMs (eg, models 2764 or 27128) using a circuit that occupies little space on a pc board **(Fig 1)**. The signal interface consists of an 8-bit control word and an 8-bit data bus.

The switching regulator (IC_3) provides the EPROM's programming voltage by stepping the 5V supply to 21V. The 12-bit binary counter (IC_1) simplifies the generation of EPROM addresses. After resetting the counter to 0 by applying a pulse to pin 11, you can step the EPROM through its addresses by applying pulses to the counter's clock input, pin 10. Refer to the EPROM data sheet for details on controlling the other inputs (O_1, O_2, and O_5 to O_7).

You can verify the contents of the EPROM against your original object code by the same process of strobing the counter for each address and reading the data bus for that address. Again, refer to the data sheet for details on reading data from the EPROM. **EDN**

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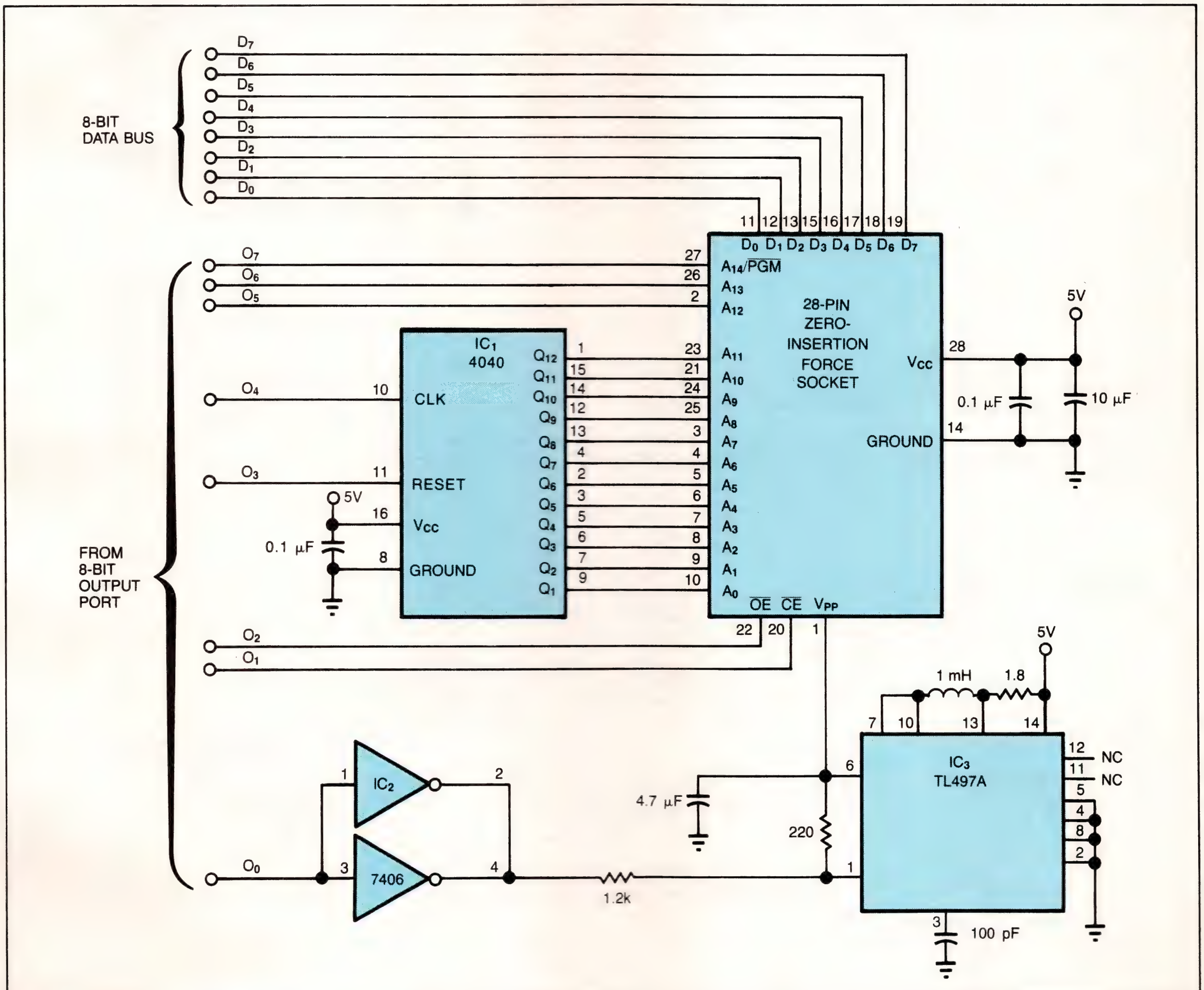

*Fig 1—****Program EPROMs using a binary counter*** *for address generation and a step-up switching regulator to supply the 21V programming voltage.*

Algorithm approximates sum of quadratures

Grimes G Slaughter
Conray Inc, Oak Ridge, TN

To calculate the magnitude of a complex frequency, you can use both hardware and software approaches. Unfortunately, you need square-root routines (which are relatively slow) to calculate the expression in software; to calculate it in hardware, you need expensive analog multipliers. However, if your application can tolerate the resulting error **(Fig 1b)**, you can approximate the expression using a simple Basic algorithm that does the job quickly.

The magnitude of a complex frequency is equal to the vector sum $(A^2+B^2)^{0.5}$ of its quadrature components

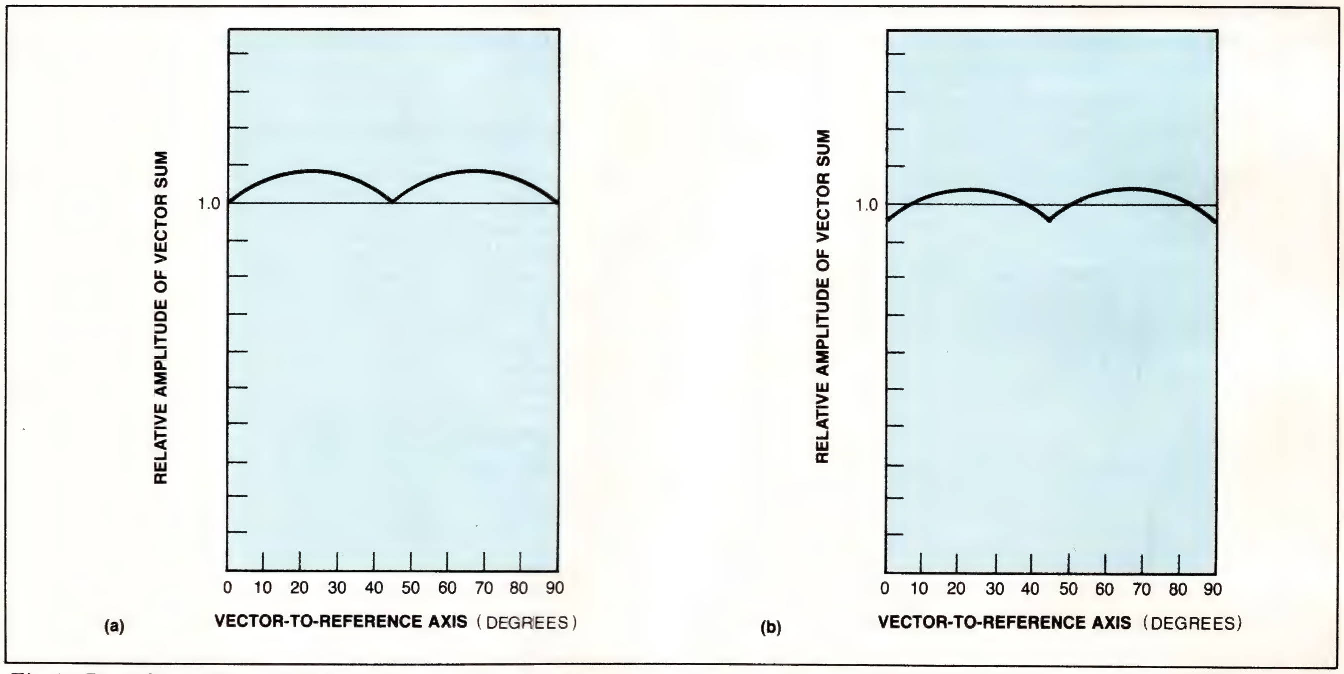

***Fig 1—Basic lines 100 and 110** in the accompanying text approximate a vector sum of quadrature components **(a)**. To improve the approximation, use lines 200 and 210 **(b)**.*

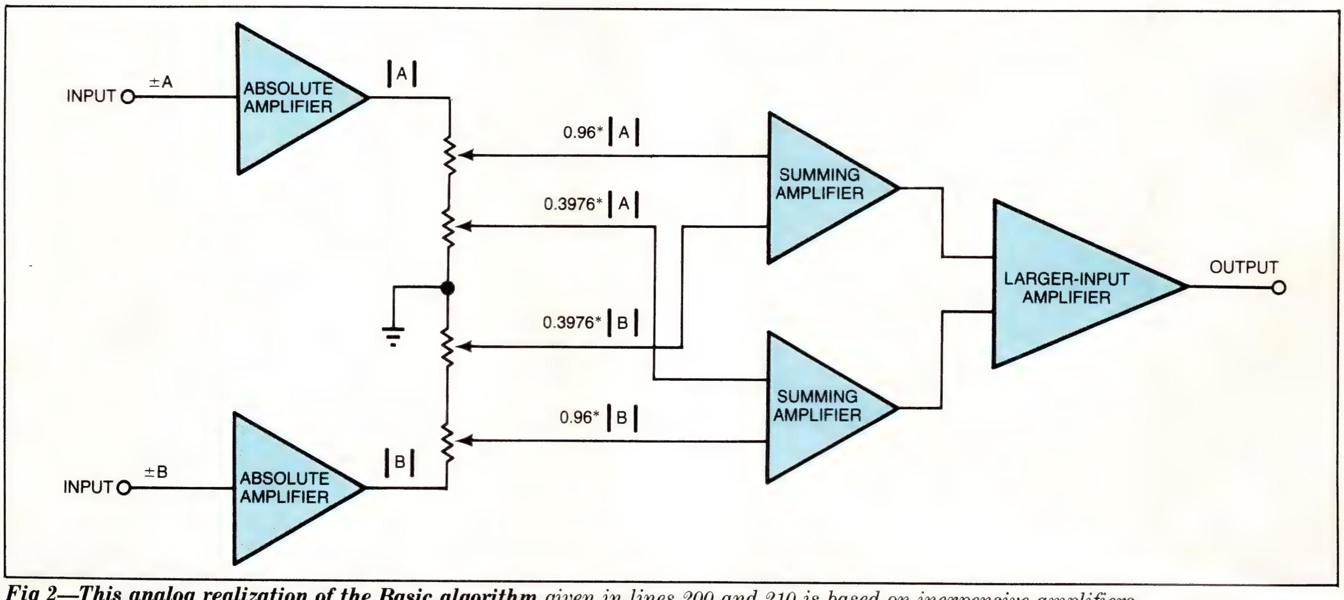

***Fig 2—This analog realization of the Basic algorithm** given in lines 200 and 210 is based on inexpensive amplifiers.*

cos(2πft) and jsin(2πft), where A and B are the magnitudes of those components. The algorithm is as follows:

```
100 C=ABS(A)+0.4142137*ABS(B)
110 IF ABS(B)>ABS(A) THEN
    C=ABS(B)+ 0.4142137*ABS(A)
```

The multiplying constant is chosen for a correct approximation (no error) when the vector sum C and the reference axis form a 45° angle. At 45° both the sine and cosine have a value of 0.7071067, so either must have a correction of (1−0.7071067), or 0.2928933, added to give the correct vector sum of unity. If K is the correction factor, then K=0.2928933/0.7071067, or 0.4132137.

The algorithm gives an approximation that is correct at 0° and at every multiple of 45° thereafter; in the algorithm's logic, the sine and cosine exchange roles at those points. **Fig 1a** shows the correct vector sum (unity) vs results using the algorithm as functions of the vector's angle with the reference axis. The maximum error (1.08239, or about 8%, occurring at 22.5°) may be halved by adding a factor of 0.96 to the algorithm expressions:

```
200 C=0.96*ABS(A)+0.3976451*ABS(B)
210 IF ABS(B)>ABS(A) THEN
    C=0.96*ABS(B)+0.3976451*ABS(A)
```

Fig 1b shows the result of this modification.

You can also implement lines 200 and 210 in hardware using inexpensive amplifier configurations as shown in **Fig 2**. You can expand the scheme by obtaining additional terms from the resistor string to achieve an error of 1 or 2%. Further, when inputs A and B are positive, you don't need the absolute amplifiers. **EDN**

To Vote For This Design, Circle No 750

Drive stepper motor without missing steps

Pieter Kleingeld
Rijksuniversiteit Utrecht, Instituut voor aardwetenschappen, Utrecht, The Netherlands

The shaft of a stepper motor should advance by one increment of angular rotation for each digital pulse you apply. As the shaft's rpm value approaches its region of mechanical resonance, however, the motor sometimes misses steps; ie, its shaft may advance by fewer increments of rotation than the number of pulses applied.

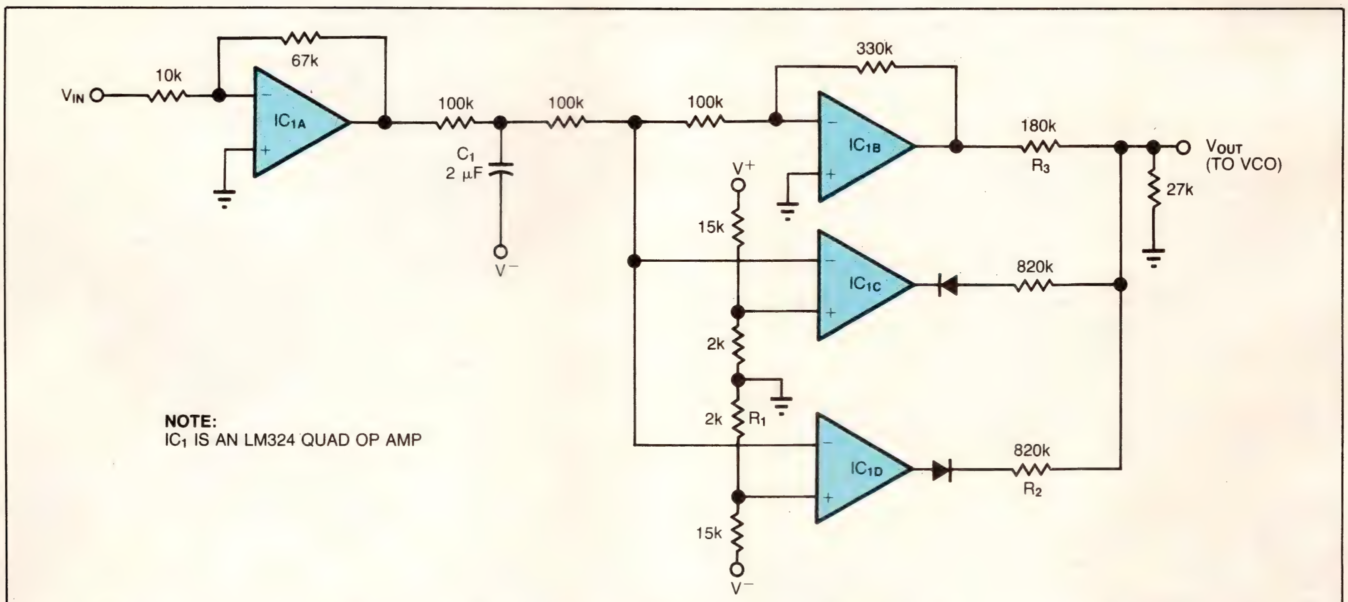

*Fig 1—**Using this circuit, you can prevent** the missing steps that result when a stepper motor is driven near its resonant frequency. The circuit avoids the corresponding inputs to the motor's VCO controller.*

For systems that use a voltage-controlled oscillator (VCO) for motor control, you can avoid missing steps by using the **Fig 1** circuit to supply the VCO input. The circuit output combines a voltage-dependent step waveform with a waveform that is linearly related to V_{IN}. The resulting transfer function **(Fig 2)** skips the output-voltage range that produces the pulse frequencies that cause the motor to resonate.

For positive values of V_{OUT}, component values R_1 and R_2 in **Fig 1** set the threshold (γ) and width (δ), respectively, of the forbidden V_{OUT} range **(Fig 2)**. R_3 sets the overall gain, V_{OUT}/V_{IN}, which is reduced for V_{IN} above or below the step thresholds.

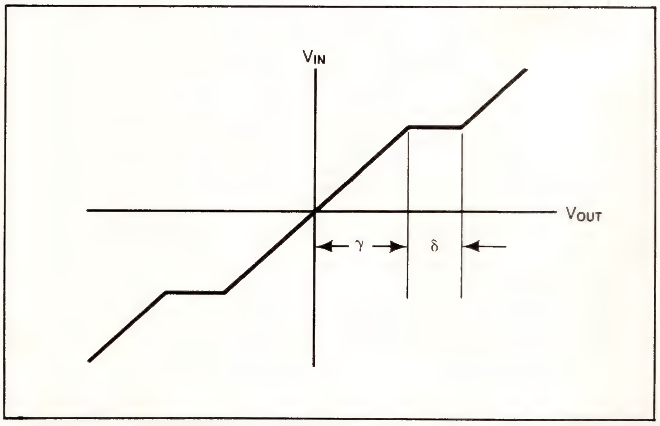

Fig 2—The circuit in Fig 1 yields this transfer function. Choose R_1 to set the V_{OUT} threshold γ and R_2 to set the V_{OUT} range δ to be excluded.

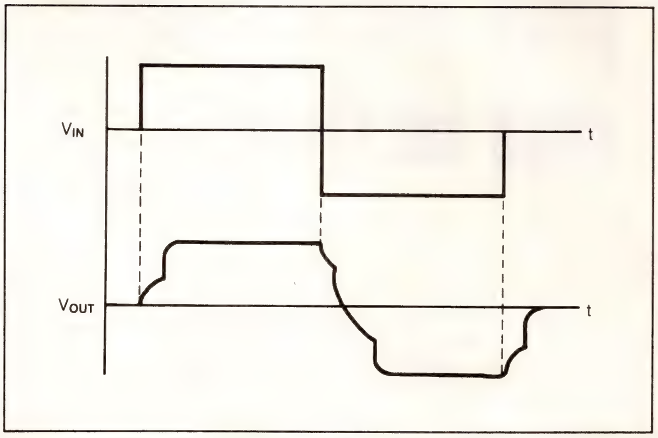

Fig 3—The dynamic behavior of the Fig 1 circuit exhibits a controlled response (set by capacitor C_1) and excludes troublesome values of V_{OUT}.

Fig 3 shows the circuit's dynamic response. You choose the value of capacitor C_1 for the desired rate of change in V_{OUT}—ie, outside its forbidden zone. (The 2-μF value shown for the capacitor is typical; in fact, all component values shown in **Fig 1** are typical.) **EDN**

To Vote For This Design, Circle No 749

Pulse generators offer improved performance

P Gascoyne
UKAEA, Culham Lab, Oxon, UK

With certain modifications and additions to a circuit **(Fig 1)** from an earlier Design Idea (Barnett, T G, "Pulse generator has variable duty cycle," EDN, October 4, 1984, pg 249), you can enhance the performance of a variable-duty-cycle pulse generator.

If only ±15V power supplies are available, it's better to attenuate the output of the duty-cycle potentiometer **(Fig 2b)** than to reduce the voltage across the potentiometer (**Fig 2a**). Either method produces the desired ±1V output range, but **Fig 2b** offers as much as a ×14 improvement in rejecting asymmetrical changes in the supply voltages.

The voltage follower IC_C in **Fig 1** is not essential for buffering the potentiometer. If desired, this op amp could instead be used to provide an inverted output. Or, using a second potentiometer, it could generate an output with a different duty cycle.

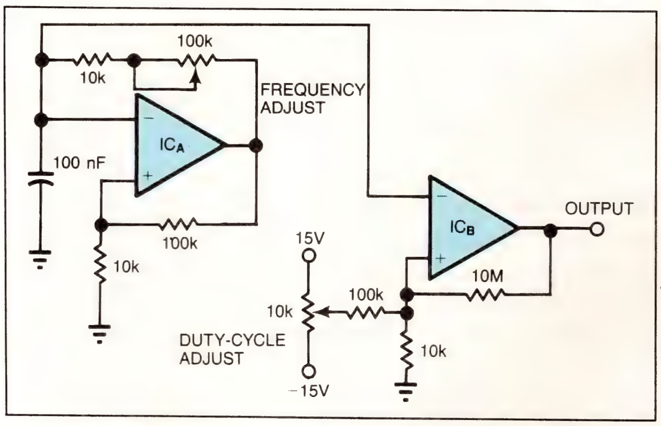

Fig 1—This pulse generator offers independent control of frequency and duty cycle, and it can be enhanced in several ways.

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Some hysteresis via positive feedback (obtained by adding 1-kΩ and 1-MΩ resistors, as shown in **Fig 3**) will improve the output stability and shorten the rise and fall times. The resistors allow a clean response for output frequencies as low as 0.02 Hz.

By replacing **Fig 1**'s 2-op-amp (IC_A and IC_B) triangle-wave generator with a generator based on one op amp, you can build an economy-version pulse generator using a dual op amp **(Fig 4).** Although **Fig 4**'s triangle waveform consists of exponential rather than linear segments, the resulting error is small because the timing capacitor charges to only 10% of maximum on each cycle. This circuit tolerates power-supply variations—a 3V change in either supply causes little effect on the duty cycle.

Finally, you can sweep or otherwise modulate the duty cycle by replacing the potentiometer with a suitable ac signal. The deluxe-version swept-pulse generator in **Fig 5** uses a second low-frequency wave generator for the sweeping. **EDN**

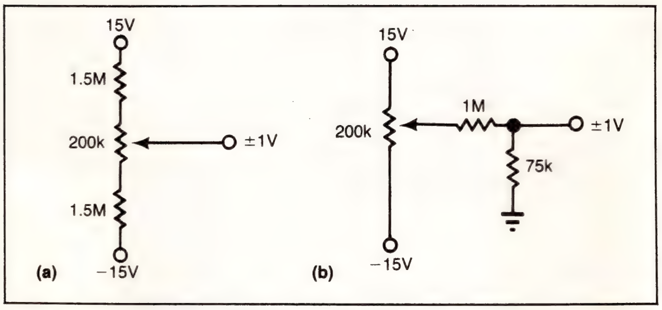

Fig 2—The divider shown in b is preferable *to that shown in **a** because it provides more rejection for asymmetrical changes in the supply voltages.*

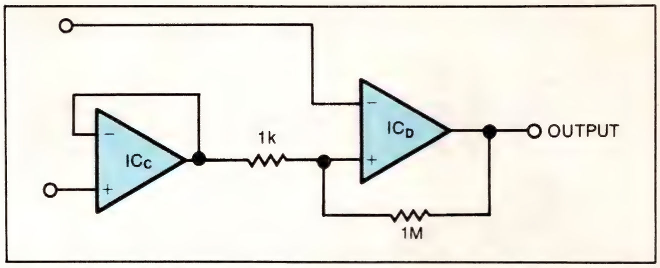

Fig 3—Improve the low-frequency response *of the output stage in **Fig 1** by adding 1-kΩ and 1-MΩ resistors to provide hysteresis.*

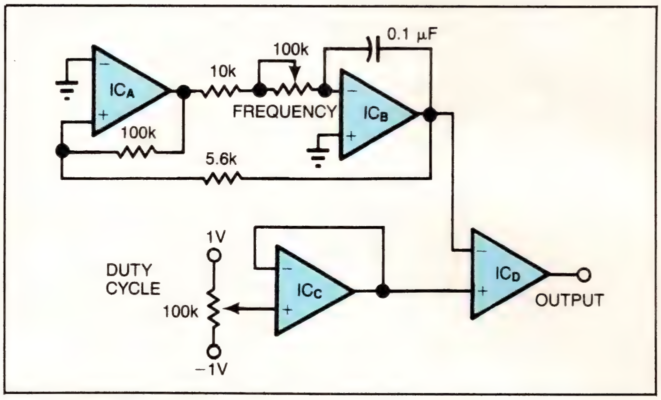

Fig 4—This pulse generator uses one dual op amp *and provides independent control of frequency and duty cycle. In addition, it tolerates an unbalance of 3V or more in the power supplies.*

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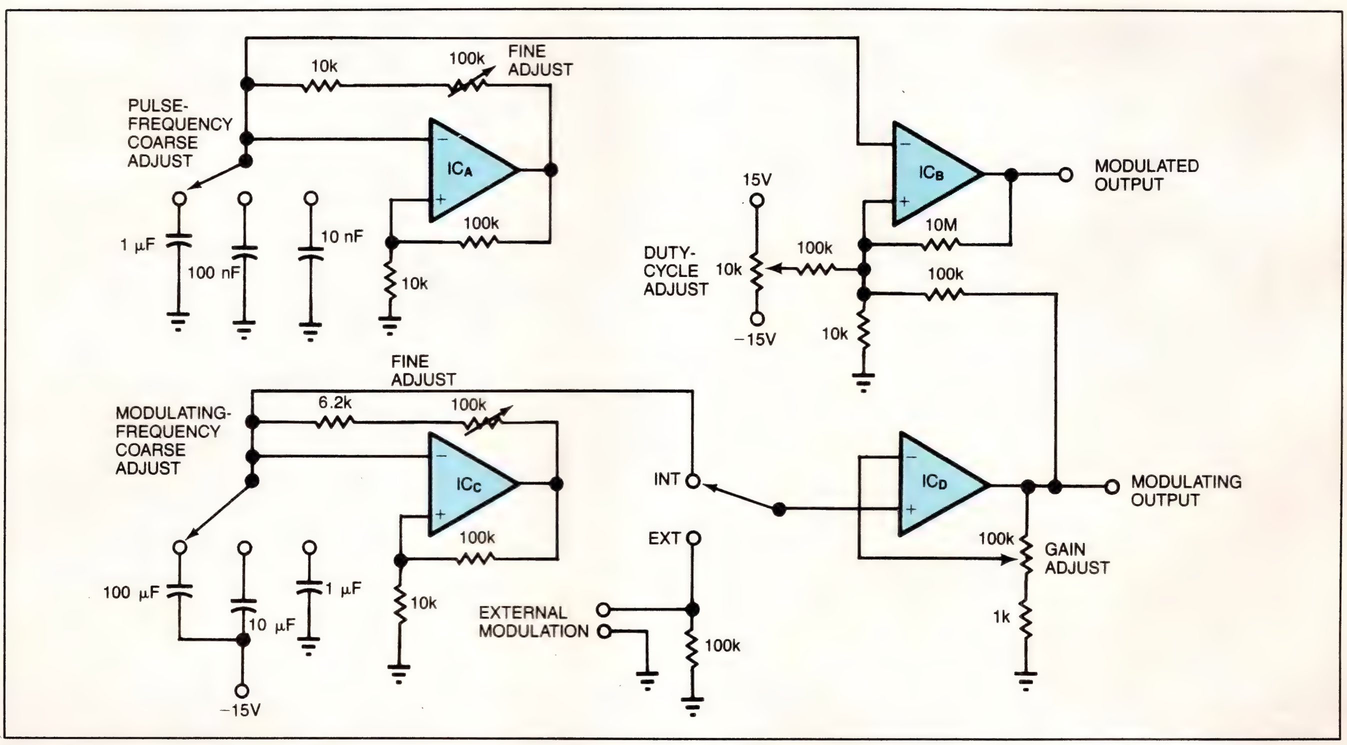

Fig 5—A deluxe version of the pulse generator *offers a swept duty cycle as an option.*

Calculator performs binary arithmetic

D G Sporea and V G Velculescu
Central Institute of Physics, Magurele, Romania

Using a binary-arithmetic program called Binarth **(Listing 1),** you can perform binary arithmetic on an HP67 or HP41 handheld calculator. The binary-arithmetic capability is useful for checking the results of programs and algorithms developed for multibyte

LISTING 1

```
f LBL A   Binary-to-decimal conversion
h CF 0
Cl x
STO 9
RCL A
f x=0
GT 04
f GSB D
RCL 5
×
STO 9
f LBL 4
RCL B
f x=0
GT 05
f GSB D
RCL 6
×
STO +9
f LBL 5
RCL C
f x=0
GT 06
f GSB D
RCL 7
×
STO +9
f LBL 6
RCL D
f GSB D
STO +9
RCL 9
h RTN
f LBL B   Decimal-to-binary conversion
h SF 0
STO 9
RCL 5
÷
f INT
STO 8
f x=0
GT 07
f GSB D
RCL 9
RCL 8
RCL 5
×
-
STO 9
RCL 1
f LBL 7
STO 8
RCL 9
RCL 6
÷
f INT
STO 8
f x=0
GT 08
f GSB D
RCL 9
RCL 8
RCL 6
×
-
STO 9
RCL 1
f LBL 8
STO B
RCL 9
RCL 7
÷
f INT
STO 8
f x=0
GT 09
f GSB D
RCL 9
RCL 8
RCL 7
×
-
STO 9
RCL 1
f LBL 9
STO C
RCL 9
f GSB D
STO D
h RTN
f LBL C
f GSB A
STO 8
R/S
f GSB A
RCL 8
h x⇄y
STO E
R/S
h ABS
h ↑
g FRAC
h STI
h ↓
f INT
f GSB B
R/S
RCL E
h RCI
×
f INT
f GSB B
h RTN
f LBL D
STO 0
Cl x
STO 1
1
EEX
1
0
STO 2
RCL 7
STO 3
h F ?
GTO 0
f LBL 1
RCL 3
2
÷
STO 3
RCL 2
1
0
÷
STO 2
RCL 0
h x⇄y
g x > y
GTO 2
-
STO 0
RCL 3
RCL 1
+
STO 1
f LBL 2
1
RCL 3
g x > y
GTO 1
RCL 1
h RTN
f LBL 0
RCL 2
1
0
÷
STO 2
RCL 3
2
÷
STO 3
RCL 0
h x⇄y
g x > y
GTO 3

STO 0
RCL 1
RCL 2
+
STO 1
f LBL 3
RCL 0
f x > 0
GTO 0
RCL 1
h RTN
f LBL E   Initiation of registers 5, 6, and 7
1
0
2
4
h ↑
STO 7
g x²
STO 6
×
STO 5
DSP 0
Cl x
h RTN
```

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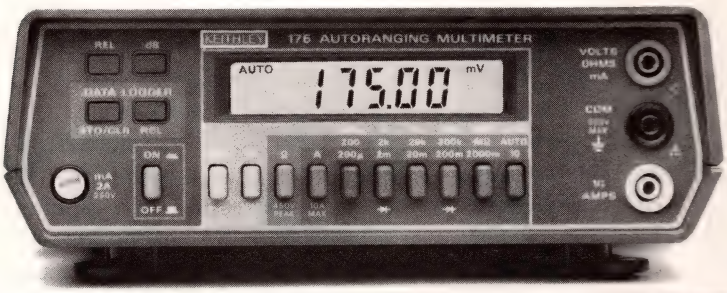
Keithley Instruments, Instruments Division, 28775 Aurora Road, Cleveland, Ohio 44139. Phone: (216) 248-0400.



Model 175 Autoranging DMM
- ☐ 4½ digits
- ☐ Data logger, relative reference, dB
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KEITHLEY

CIRCLE NO 85

arithmetic in microprocessor systems. The program is based on software routines that appeared in an earlier Design Idea (Talmor, Shlomo, "Convert binary/decimal numbers," EDN, February 9, 1984, pg 228).

The Binarth program performs addition, subtraction, multiplication, and division for binary numbers as long as four bytes. The operands are introduced in binary form. The results are presented in binary, but the intermediate operations are performed in decimal format. Operands and results must not exceed $2^{32}-1$.

In operation, subroutine LBL E (line 180) generates and stores the first, second, and third powers of 1024, a base number (2^{10}) that is compatible with the 10-digit calculator display.

Subroutine LBL A (line 1) converts a binary number to its decimal equivalent. You partition the binary number into 10-bit groups, beginning with the LSB. For a maximum-length 32-bit number, the partitioning leaves only two bits in the last (most significant) byte. Next, enter each byte into the calculator, from right to left, as in the following example:

10 0011000100 1111110001 0110001100

Key in 110001100- STO D, 1111110001- STO C, 11000100- STO B, 10- STO A. Then press key A to display the result in decimal form: 2354038156.

In contrast to subroutine LBL A, subroutine LBL B (line 34) converts a decimal number to binary form. To convert 2354038156, for example, enter the number into the calculator and press key B. You obtain the result via the calculator's RCL function (but you must add the required number of zeros to the right side of each group so that each contains 10 digits):

RCL A- 10
RCL B- 0011000100
RCL C- 1111110001
RCL D- 0110001100

The program uses subroutine LBL C (line 91) to convert binary operands to decimal (by calling LBL A); the program then executes the required arithmetic operation on the decimal numbers and converts the result to binary by calling LBL B. **EDN**

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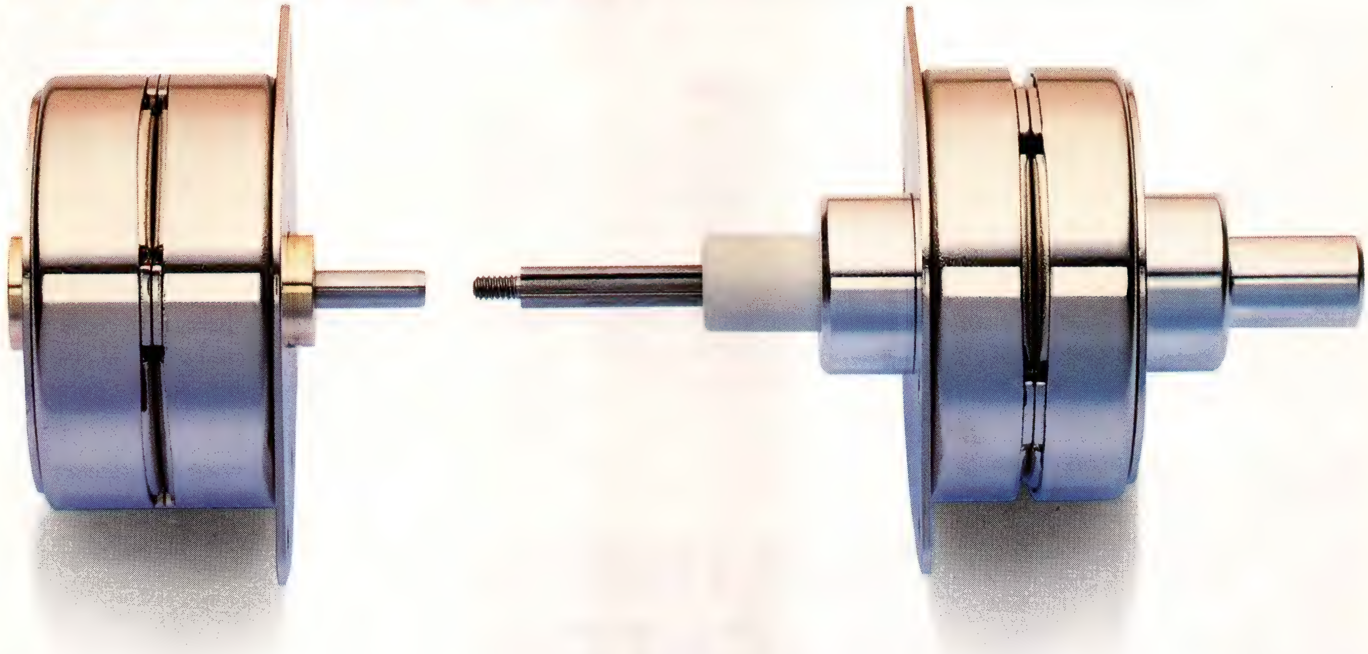

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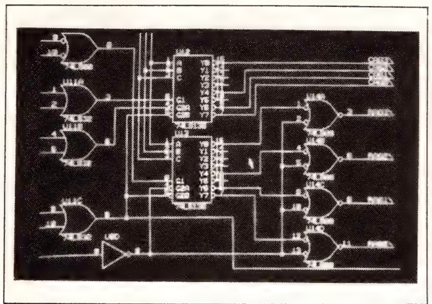


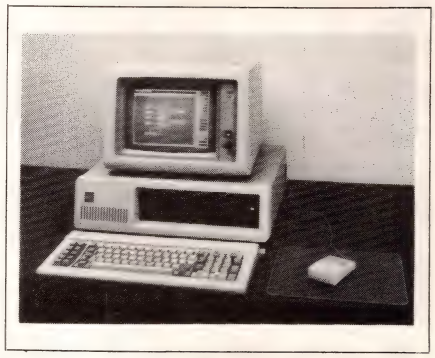
SCHEMATIC DESIGN

Running on an IBM PC or compatible computer, this company's /SDT schematic-capture program allows you to place parts, wires, text, and other objects on a screen via keyboard or mouse commands. You can move, rotate, replicate, and delete selected parts. Possible worksheet sizes range from A to E. The package features hierarchical schematic organization and rubberbanding of wires, buses, and blocks. An on-line, 1200-part library contains TTL and CMOS devices, memories, discrete components, μPs, and peripherals. You can suspend a session and switch to DOS command execution. The package provides four utility programs: schematic-output generation, net-list creation, design checking, and a bill-of-materials file. It requires MS-DOS, version 2.0 or higher, a 360k-byte floppy-disk drive, and 256k bytes of RAM. $495.

OrCAD Systems Corp, 23315 W Baseline Rd, Hillsboro, OR 97123. Phone (503) 640-5007.

Circle No 350

PLD DESIGN



You can use Vista to design schematics on an IBM PC, PC/XT, or PC/AT and translate the design into a format that you can program into a standard PLD. It uses an optical mouse for schematic input and interfaces to either a 640×400-pixel color-graphics display (16 colors) or a 640×200-pixel monochrome-graphics display. The package includes Assisted Technology's CUPL compiler. After you have entered your schematic, the package creates a net-list file and passes that file to the CUPL program for compilation, simulation, and verification. Finally, the compiler translates the schematic to a standard JEDEC file with test vectors. The company's 160 Universal Memory/Logic Programming System can use the JEDEC file to program PLDs. The package can interface with Data I/O, Stag, Kontron, and other programmers.

$3395 (without graphics card).

Valley Data Sciences, 2426 Charleston Rd, Mountain View, CA 94043. Phone (415) 968-2900. TLX 4993461.

Circle No 351

TEST MANAGER

The Boardwatch software system collects and analyzes board-test data. It interfaces with its manufacturer's L200 Series VLSI board testers. The package features a paperless repair system that automates the collection and analysis of test, diagnosis, and repair data. To use this software, you enter the serial number of each board that you test and relay the serial number, along with the test results for that board, to the system. If the board fails its tests and requires further diagnosis, you send the board to a diagnostic station, where you enter the board's serial number once more and relay that number to the test manager. The package includes a relational-database manager, a utility that controls an operator's access to test systems, a utility for monitoring tester use, and L200-system interfaces to a LAN. You can modify standard report formats or create new ones. You can store, catalog, and update all jobs on any VAX. Conversely, users of L200s can use their terminals to access the package on a VAX. $75,000 to $200,000, depending on the number of L200 test systems on a network. Deliveries to begin in mid-1986.

Teradyne Inc, 321 Harrison Ave, Boston, MA 02118. Phone (617) 482-2700. TWX 710-321-1055.

Circle No 352

FAULT SIMULATOR

This fault simulator, Megafault, is an enhanced version of the Daisy Megalogician fault simulator. A concurrent algorithm and a hardware accelerator increase the speed of the package's fault simulations. For example, this unit evaluated a 10,000-gate fault simulation in a few hours; on a VAX 11/780, the same process required a day of computation. The fault simulator uses the same models and test vectors as the Megalogician. $45,000.

Daisy Systems Corp, 700 Middlefield Rd, Mountain View, CA 94043. Phone (415) 960-0123.

Circle No 353

ANALOG DESIGN

The Analog Designer brings CAE to analog boards and circuits. It runs a set of software analog-design instruments that help you validate your designs. These software instruments consist of mock-ups of a digital voltmeter, an oscilloscope, a network analyzer, and a function generator. The instruments use

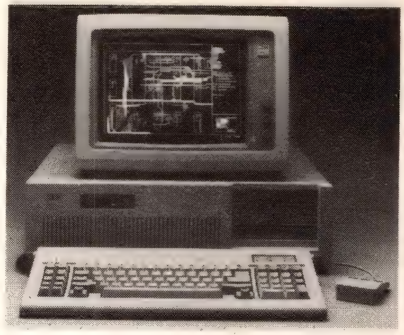
ValidSpice for modeling circuits. You select your software instruments from a menu on the company's workstation. Prices start at $79,000; to upgrade an existing Scaldsystem costs $25,000.

Valid Logic Systems Inc, 2820 Orchard Parkway, San Jose, CA 95134. Phone (408) 945-9400.

Circle No 354

PC-BOARD LAYOUT

Because the CT2400 pc-board layout system uses the same set of commands as this company's other CAE products, you can learn how to use this layout package quickly. The pc-board layout program provides automatic placement and packaging of components. The router displays connections among all components.



Component interconnections move in a rubberbanding style when you move components. Both 45 and 90° angles are available. Using this program, you can identify critical gates during schematic design. The program then automatically packages the remaining gates for maximum design efficiency. During pc-board layout, the program's interactive design-rule checkers point out any rule violations. Back annotation furnishes documentation and schematic hard copy. The program runs on IBM PC/ATs under the PC-DOS operating system. $4250.

Case Technology Inc, 633 Menlo Ave, Menlo Park, CA 94025. Phone (415) 322-4057. TLX 506513.

Circle No 355

DESIGN AND TEST SET

TestEdge is a set of simulation and testing tools that allows you to create fully testable designs. The set includes a simulation and test language (STL), testability analysis tools, and a graphical fault-simulator interface. STL's simulation output-comparison feature lets you model the behavior of your circuit and compare the simulation results of a logical model and a behavioral model. The package interfaces with Simucad's Silos logic and fault simulator, Spice circuit simulators, and the Sentry tester. The software is offered as an option to this company's IC design systems. $16,500.

SDA Systems, 2461 Mission College Blvd, Santa Clara, CA 95054. Phone (408) 727-7811.

Circle No 356

3 MORE KEPCO/TDK SWITCHERS PROVE THAT LOW-PRICED DOESN'T HAVE TO MEAN CHEAP.

Our popular Series MRM — compact, multi output, PC Card switching power supplies for the logic, display, communications, and disk drive requirements of CRT terminals and microcomputers — now has five TÜV-certified members. The power range of the series has been extended to 120 Watts, as the 40-Watt MRM 144KV and the 60-Watt MRM 250KV are joined by the 80-Watt MRM 260KV and the 120-Watt MRM 270KV and MRM 280KV.

Like all Kepco/TDK switching power supplies, their prices are surprisingly low. But they offer all the most-needed features and possess all these well-known Kepco/TDK hallmarks of quality:

Hybrid microcircuits, designed and manufactured in-house, provide control, OVP, current limit, and start-up functions. They greatly reduce parts count and improve MTBF.

8mm primary-secondary, 4mm primary-to-ground spacing for the safety requirements of IEC 380/VDE 0806. All these power supplies have been certified by TÜV Rheinland, and are UL Recognized, CSA Certified.

Transformers of TDK H7C1 ferrite meet the 3750V withstand test of VDE 0806/IEC 380. All chokes also have TDK H7C1 cores.

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105°C input capacitors, which store enough energy for at least 20 milliseconds holding time.

Input filters of our design and manufacture attenuate conducted EMI below FCC 20780 Class B.

All components mounted on PC board by machines developed in-house.

MODEL	MRM 144KV	MRM 250KV	NEW! MRM 260KV	NEW! MRM 270KV	NEW! MRM 280KV
a-c input	115/230	115/230	115/230	115/230	115/230
d-c outputs					
+5V	0.45-5.0A[1]	2.0-6.0A (I_1)[2]	3.0-8.0A	3.0-15A	3.0-11A
+12V	0.3-2.5A[1]	0.5-3.0A (I_2)[2]	0.5-3.0A	0.5-5.0A[3]	0.5-5.0A
−12V	0-0.5A[1]	0-1.0A	0-0.7A	0-0.7A	0-0.5A
−5V	—	0-0.5A	0-0.3A	0-0.3A	—
+24V	—	—	—	—	0.3-1.3A (1.7A peak)
Prices *	$80	$99	$130	$185	$185

(1) The maximum combined power for all three outputs is 40W (0-50°C).
(2) Maximum current, $I_1 + I_2$ = 8A. (3) 8.0A peak.
* Substantial OEM discount available.

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CIRCLE NO 89

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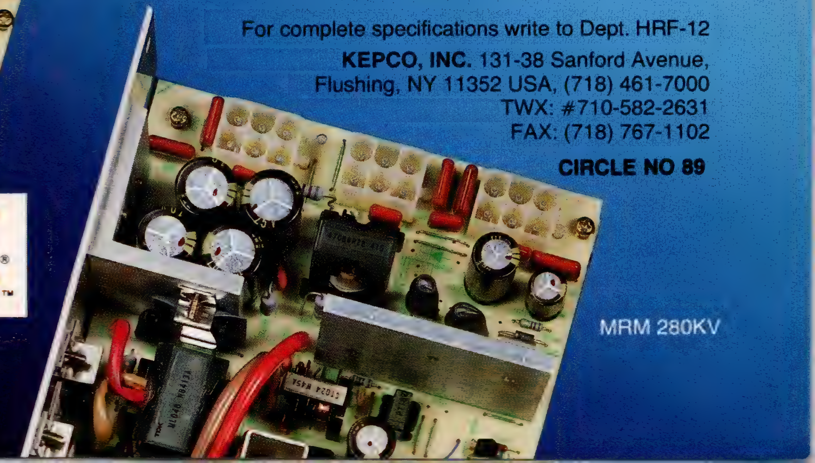
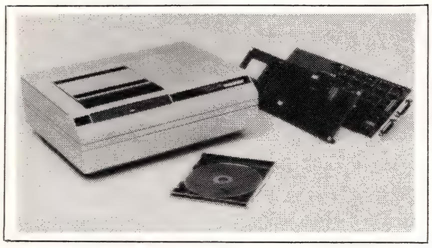


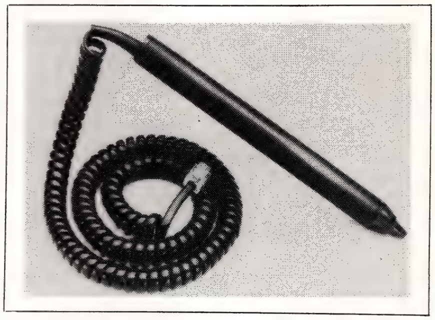


DISK READER

If you have a DEC Rainbow, IBM PC, or compatible computer, you can use a CD Massfile to access large databases. It reads removable compact disks (CDs) that are prerecorded with information in a Uni-File data format. The unit lets you access permanent data stored in large read-only databases such as encyclopedias, dictionaries, catalogs, and technical manuals. Each optical CD can hold 550M bytes of information, equivalent to 250,000 single-spaced typed pages or 1600 5¼-in. floppy disks. The CD Massfile includes a CD reader, a controller board that supports as many as two readers, and diagnostic software. A lighted panel on the reader provides power-on, activity, and error indications. $1695; each controller card, $295.

Tecmar Inc, 6225 Cochran Rd, Solon, OH 44139. Phone (216) 349-0600. TLX 466692.

Circle No 357



LIGHT PEN

The FT-176 light pen provides an optical user interface for monochrome displays. This light pen's circuitry overcomes the problem of long-persistence phosphor that made previous pens incompatible with monochrome displays. You can also use the light pen with color monitors. When used as a pointing device, it simplifies menu selections and windowing tasks on a personal computer. $235.

FTG Data Systems, Box 615, Stanton, CA 90680. Phone (714) 995-3900. TLX 887840.

Circle No 358

DAISY-WHEEL PRINTER

The $399 KX-P3131 daisy-wheel printer accommodates proportional spacing, impression intensity, automatic justification, superscript, and subscript printing. The printer uses Diablo 630 ribbons and 96-character plastic print wheels and prints 17 cps. It offers word-processing features like centering, bold print, shadow, outline, and single and double underlining. You can select char-

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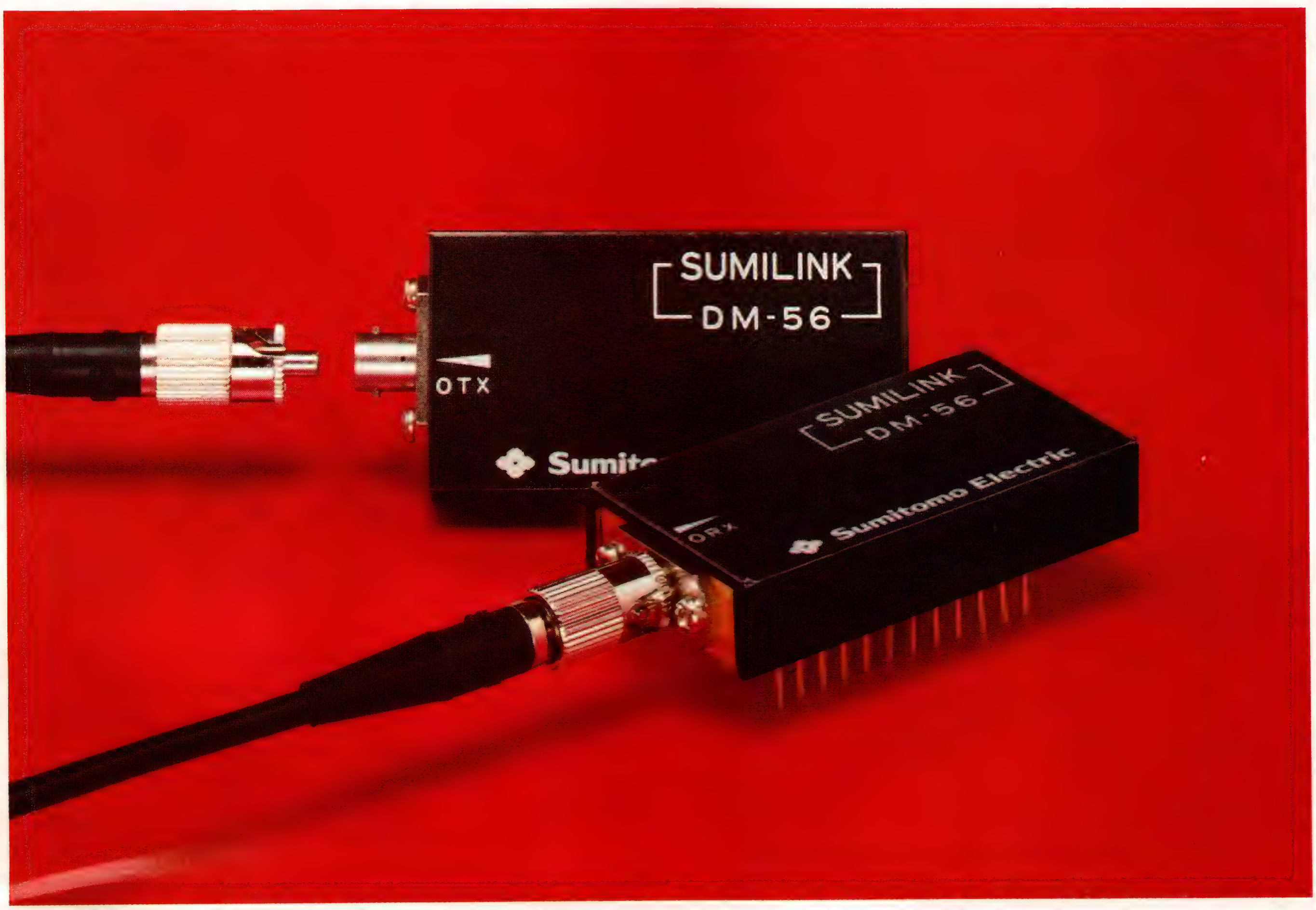

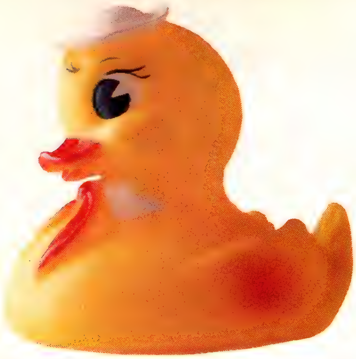

Bt101. Triple 8-bit VIDEODAC, 50 & 30 MHz, Monolithic, +5v CMOS, 40-pin CERDIP.

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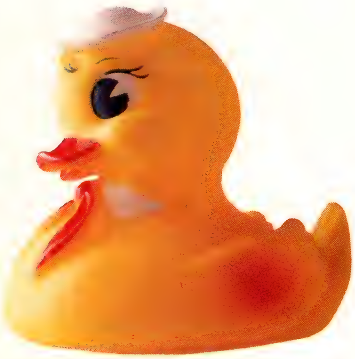
Bt103. Triple 4-bit VIDEODAC, 75 & 30 MHz, Monolithic, +5v CMOS, 28-pin CERDIP.



Bt104. 12-bit DAC, 35 ns Settling, Monolithic, +5v CMOS, 20-pin 0.3″ CERDIP.

Bt105. 12-bit DAC with latch, 35 ns Settling, Monolithic, +5v CMOS, 20-pin 0.3″ CERDIP.

Bt106. 8-bit VIDEODAC, 50 & 30 MHz, Monolithic, +5v CMOS, 20-pin 0.3″ CERDIP.

Bt444. 4-bit VIDEODAC, 40 MHz, Hybrid, +5v CMOS, Pin-compatible VDAC 444TD.

Bt452. 4-bit RAMDAC, 16 x 12 Color Lookup Table, 40 MHz, Hybrid, +5v CMOS, Pin-compatible to RGB DAC 4TD.

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Panasonic Industrial Co, Computer Products Div, 1 Panasonic Way, Secaucus, NJ 07094. Phone (201) 348-7183.

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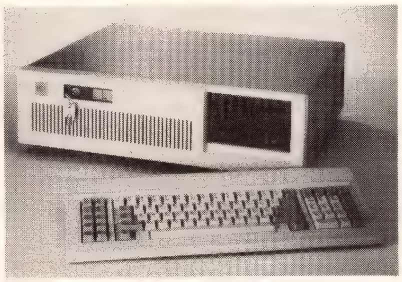
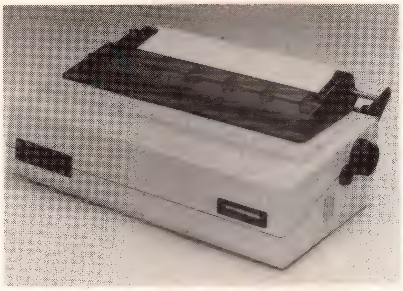


COMPUTERS

The Fast Series of computers offers IBM PC/AT compatibility and a host of standard features. Fast-1 comes with 640k bytes of RAM, a 1.2M-byte 5¼-in. floppy-disk drive, a speaker, a 200W power supply, 64k bytes of ROM, eight I/O expansion slots, a clock/calendar with battery backup, a key lock, an 84-key keyboard, a controller card, and a socket for an 80287 math coprocessor. Fast+ adds a 20M-byte hard-disk drive, a serial port, and two parallel ports. Both computers are available with 1M byte of onboard RAM; expansion boards let you configure the systems with as much as 16M bytes of RAM. Fast-1, $2500; Fast+, $3000.

Innovative Computer Technology Inc, 30 Broad St, Denville, NJ 07834. Phone (201) 586-2600.

Circle No 360

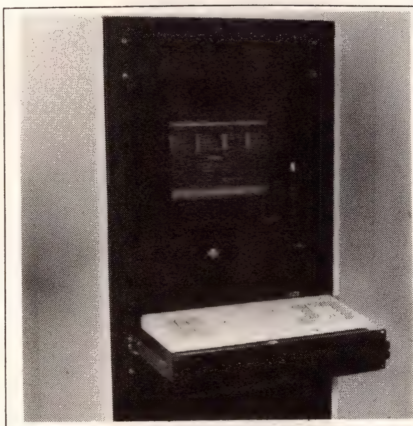


SERIAL MATRIX PRINTER

Featuring interchangeable font cartridges, the MT290 serial matrix printer also gives you a choice of paper-feed methods. The printer includes both tractor- and friction-feed mechanisms for rear and bottom feeding of continuous-form paper, multiple-part forms, or single sheets. The adjustable tractors can accommodate paper widths from 3 to 16 in. Optionally, you can use the printer's automatic front-feed mechanism for cut sheets of paper without removing the continuous-form paper from the tractor mechanism. The printer prints 200 cps in draft mode or 50 cps in correspondence mode. The plug-in print cartridges include Courier, Helena, letter Gothic, italic, and modern fonts. The printer comes with a parallel interface, but optional RS-232C, current-loop, and IEEE interfaces are available. $895; with automatic front feed, $1149.

Mannesmann Tally Corp, 8301 S 180th St, Kent, WA 98032. Phone (206) 251-5500. TLX 320200.

Circle No 361



COMPUTER

The 6170 computer, a rugged version of the IBM PC/AT, uses an 80286 processor operating at 8 MHz and is 30% faster than IBM's 7532 industrial computer, according to the manufacturer. The computer al-

lows either software or hardware selection of 6- or 8-MHz operation. Its 12 expansion slots accommodate either PC/AT- or PC/XT-compatible boards. The computer comes with a 200W international power supply; a 250W supply is optional. Housed in a metal, rack-mountable 19-in. enclosure, the computer has dual cooling fans for operation to 122°F. You can add as many as three disk drives, including 360k- or 1.2M-byte floppy-disk drives and 10M- to 44M-byte Winchester drives. Options include a tape-drive backup, 2M bytes of bubble memory, and nonvolatile EPROM expansion. The front panel locks to prevent unauthorized access to the power and reset buttons and the disk drives. From $4000.

ISI International Corp, 1275 Hammerwood Ave, Sunnyvale, CA 94089. Phone (408) 743-4300. TWX 910-339-9369.

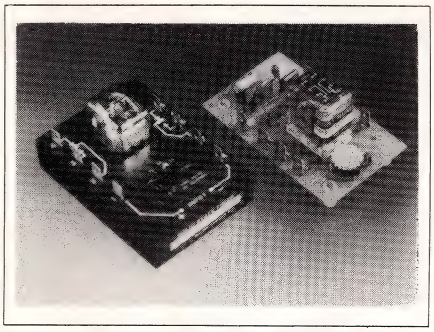
Circle No 362

STREAMING-TAPE DRIVE

The Roadrunner is a ¼-in., half-height streaming-tape drive that stores 60M bytes of data for disk backup. The drive comes with a standard QIC-36 interface. Its single-axis head-positioning mechanism eliminates head-registration problems, facilitates QIC-24 format implementation, and provides reliable cartridge interchanging among drives. An automatic gain control ensures correct data recognition. If your application requires start/stop capability, you can override the standard streaming-tape mode. The drive uses low-power CMOS circuitry and a brushless dc motor for 20W power consumption at a 100% duty cycle. Its dimensions are 5.25×8×1.63 in. Less than $500 (1000).

North Atlantic Industries Inc, Peripheral Products Div, 60 Plant Ave, Hauppauge, NY 11788. Phone (516) 582-6060.

Circle No 363

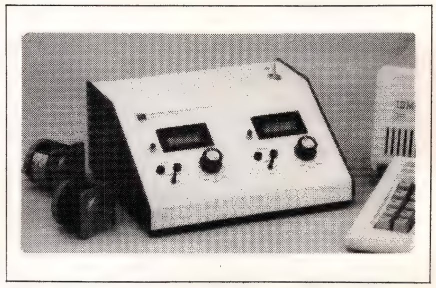


TIME-DELAY RELAYS

The ERD and OR Series time-delay relays are designed to eliminate the need for hand wiring during board assembly. The ERD Series features digital timing circuits and plastic housings. The dpdt output has a 10A rating. You can order the relays with remote adjustment, onboard adjustment (knob and dial), or with a fixed delay. Time delay ranges from 100 msec to 15 minutes, and repeat accuracy specs at ±0.5%. These devices are available in delay-on-make, interval, and single-shot versions. The OR Series units feature an open board construction and use an analog timing circuit. The output relay (spdt or dpdt) has a 10A rating. Delays range from 50 msec to 5 minutes, and repeat accuracy specs at ±2%. ERD Series, $15.64; OR Series, $12.83 (500).

SSAC Inc, Box 395, Liverpool, NY 13088. Phone (315) 622-1000.

Circle No 364



MOTOR CONTROLLER

The SMC-202A provides computer or manual control of one or two stepping motors and comes in a sloped-front cabinet that includes all necessary power supplies, motor drives, and an RS-232C interface. Both rack-mount and circuit-board versions are available. A μP controls motions, including acceleration and deceleration ramping, stored-program control, relative and absolute positioning, and automatic backlash compensation. The RS-232C port and an optional GPIB/IEEE-488 bus allow simplified interfacing to computers, controllers, and terminals. Programming commands are single-letter mnemonic codes. Manual control features include a front-panel momentary toggle switch to run the motors, a front-panel speed control to adjust the stepping rate, and an optional joystick control to provide remote manual control of the two axes. Optional digital displays allow you to monitor the motors' positions at all times. $995 (single-motor drive);

THE FASTEST SAMPLE-AND-HOLD AMPS IN THE GALAXY? AS FAR AS WE KNOW, YES!

Galaxy's Fastest: HA-5330

This sample-and-hold's acquisition time: 0.5 μs to 0.01%! That beats all other monolithics known to man. It also includes a 90pF hold capacitor dedicated to high-speed performance. Impressive specs:

- Acquisition time: 0.5 μs
- Droop rate: 0.01 $\mu V/\mu s$ (fixed) (No external hold capacitor)
- DC gain: $2x10^7$ V/V
- Aperture time: 20 ns
- Hold step error: 0.5 mV, adjustable to zero

Performance Leader: HA-5320

For a wide range of 12-bit high-speed data acquisition systems: acquisition time, 1.0 μs to 0.01%. It includes an internal 100pF hold capacitor with the option to add capacitance externally. Impressive specs:

- Acquisition time: 1.0 to 5 μs
- Droop rate: .05 to .005 $\mu V/\mu s$ (For 0pF to 1000pF of added capacitance)
- DC gain: $2x10^6$ V/V
- Aperture time: 25 ns
- Hold step error: 1.0 mV

Universal: HA-2420 & HA-2425

Add an external hold capacitor and HA-2420 or HA-2425 becomes a high-performance sample-and-hold amp with acquisition time of 3.2 μs to 0.01% or extremely low droop rate (for slower operation). Impressive specs:

- Acquisition time: 3.2 to 500 μs
- Droop rate: .005 to .000005 $\mu V/\mu s$ (For 1000pF to 1,000,000pF of added capacitance)
- DC gain: $5x10^4$ V/V
- Aperture time: 30 ns
- Slew rate: 7V/μs

All three members of the Harris sample-and-hold amplifier family can operate at gains greater than 1, eliminating the need for external scale amplifiers in many cases. In addition, they are specified for operation with ± 15 Volt supplies, but they work well from ± 12 Volts to ± 18 Volts. Options include 14-pin dual-in-line or 20-pin surface-mount packaging plus either military or commercial temperature ranges. Applications include: automatic offset zeroing, peak detector, de-glitcher, gated op amp, and input conditioner for a wide range of analog-to-digital converters.

For information contact Harris/MHS Semiconductor Sales Ltd., Eskdale Road, Winnersh, Wokingham, Berks, RG11 5TR, England.

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HARRIS

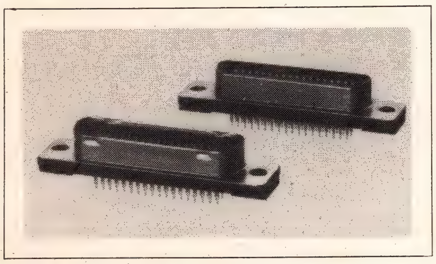
For your information, our name is Harris.

CIRCLE NO 68

$1170 (2-motor drive).

Maxwell Electronics Inc, Dept C, Box 12033, Research Triangle Park, NC 27709. Phone (919) 846-1633.

Circle No 365

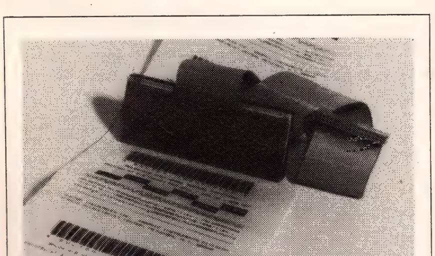


CONNECTORS

Series 266 IEEE-488 shielded pc-board connectors are available with 0.125- and 0.17-in. tail lengths. They are preassembled to ease board installation. A plug version is available in grid patterns measuring 0.085×0.151 in. or 0.085×0.160 in.; a receptacle version comes in 0.085×0.169-in. or 0.085.×0.160-in. patterns. Both versions are available in 24-, 36-, and 50-position versions. You can choose from a variety of screw-lock hardware kits and grounding straps, depending on your application. The connectors feature copper-alloy contacts with selective gold-over-nickel plating on the mating end and tin on the tail. 36-position connector, $2.14 (5000).

Winchester Electronics, Main St and Hillside, Oakville, CT 06799. Phone (203) 755-5000.

Circle No 366



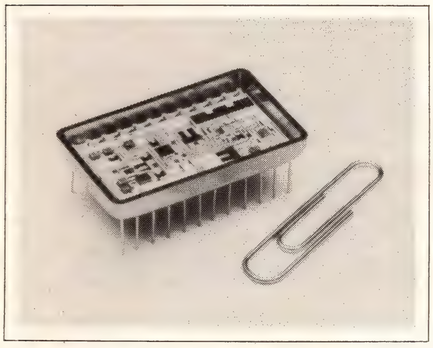
THERMAL PRINT HEADS

Onboard electronics for the SM-Series of thermal print heads include double-latched printer inputs. Suitable for graphics applications, the devices print on a thermal roll or label stock, or print through thermal transfer ribbon onto plain paper. Printing time is 4 msec per cycle (2 msec on; 2 msec off) for dot densities as high as 102 dots per in. and speeds as high as 4 in./sec. The dot line is along the substrate edge for early last-line visibility. Other features include thick-film construction, a factory-replaceable protective bar in front of the resistive printing element, and HVI²L 32-bit IC drivers. Thermistor preheaters are optional. A minimum thermal life of 50×10^6 dot lines is guaranteed. The units are ready to use with an integral heat sink and connector-terminated PVC cable. $160

to \$400. Delivery, 90 days ARO.

Gulton Industries Inc, Graphic Instruments Div, Gulton Industrial Park, East Greenwich, RI 02818. Phone (201) 548-6500. TWX 710-387-1500.

Circle No 367



HYBRID T/H AMPLIFIER

Suitable for throughput rates as high as 5 MHz, the hybrid THA-05210 track/hold amplifier offers a 150-nsec acquisition time to ±0.01% of full scale for a 10V step. It also conforms to the reliability requirements of MIL-STD-883C. Other electrical performance figures include a 0.005% linearity error, 60-psec aperture jitter, 74-dB feedthrough attenuation, a room-temperature droop rate of 0.5 μV/μsec, and a 16-MHz small-signal bandwidth. Operating ranges of −25 to +85°C and −55 to +125°C are available. The circuit consists of a unity-gain inverting op amp with series and shunt switches at its summing point. Placing the device in the hold mode opens the series switch and closes the shunt switch; placing it in the track mode has the opposite effect. While in hold mode, the analog output is held constant by the hold capacitor at the value just prior to the opening of the series switch. The THA-05210 is pin compatible with the HTC-0300A and TP4860 but uses fewer internal components than these hybrid units. Full military version, \$179 (100). Delivery, stock to eight weeks ARO.

ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

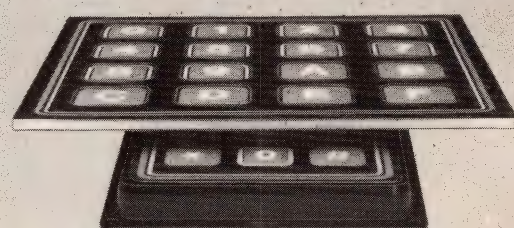
Circle No 368

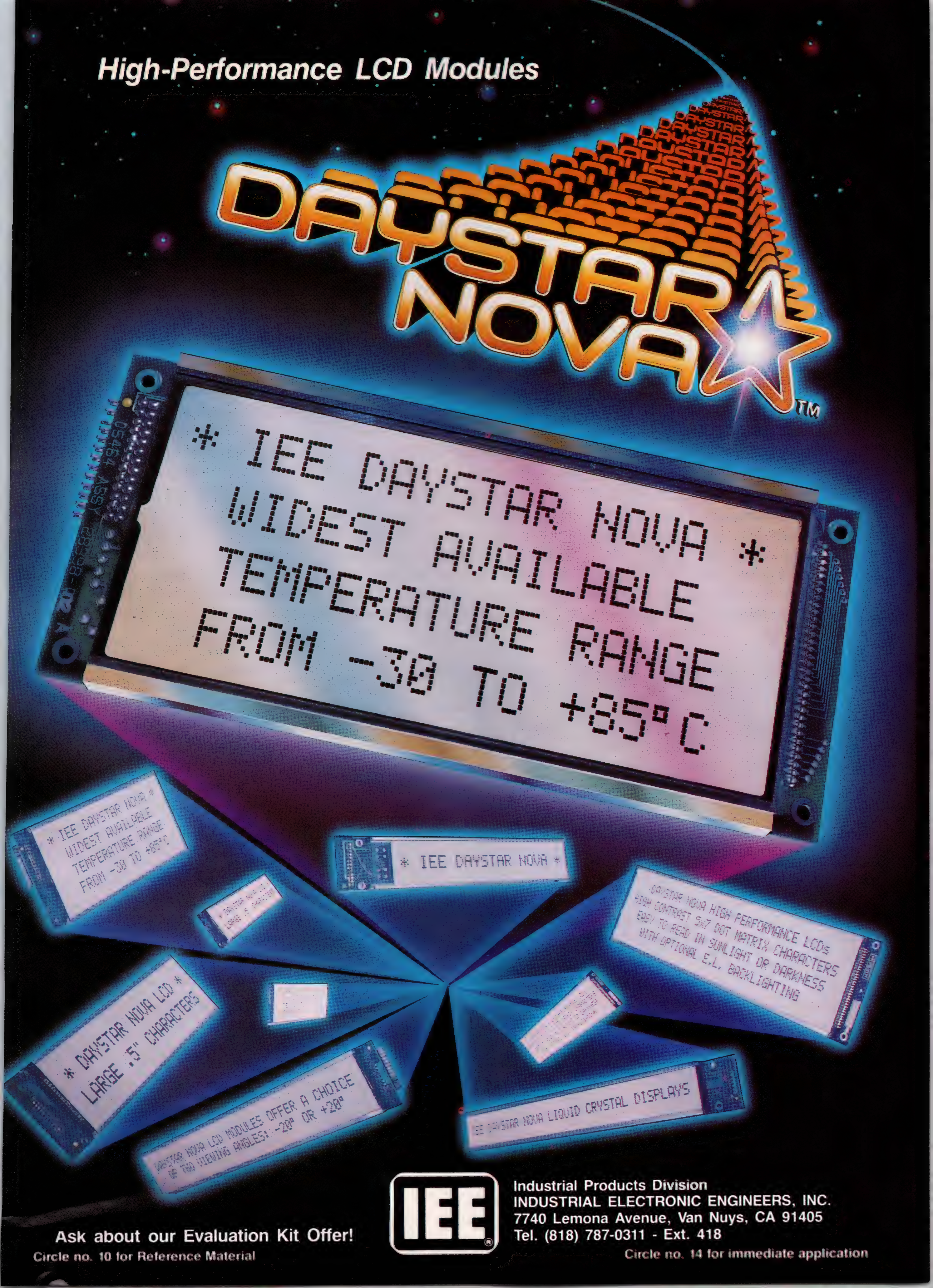
SMART DISPLAY

The HPDFL-1414 is a red, 0.112-in., 4-character monolithic alphanumeric display that combines built-in RAM, ASCII decoders, and LED drive circuitry. It features electrostatic-discharge protection furnished by large input-protection diodes, an access time of 160 nsec at 25°C, and full TTL compatibility. The device is wave solderable and is specified for operation over −40 to +85°C. \$16.35 (1000).

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 369

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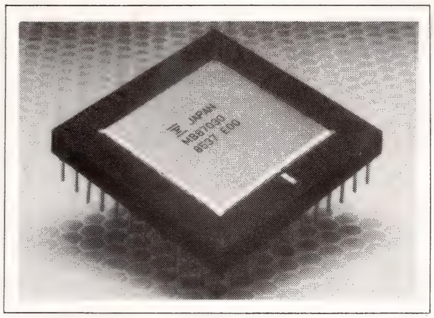


SCSI CONTROLLER

This company claims that the MB87030 is the first SCSI chip to support ANSI X3T9.2 (Revision 10) standards and to operate in synchronous and asynchronous modes. In the synchronous transfer mode, its maximum throughput rate is 4M bytes/sec. The single-chip LSI controller can replace 30 to 50 TTL and memory devices, and it can operate as a transmitter or receiver. It handles synchronous data transfer with a programmable offset of 8 bytes max and in four selectable speeds to 4 MHz. Standard SCSI protocols and procedures are built-in. The device has an 8-byte FIFO buffer and a 24-bit counter that keeps track of byte counts, phase-control logic, arbitration, and selection logic. In addition, it has provisions for single-ended and differential connections. In an 88-pin pin-grid-array package, \$35 (1000).

Fujitsu Microelectronics Inc, Integrated Circuits Div, 3320 Scott Blvd, Santa Clara, CA 95054. Phone (408) 727-1700. TWX 910-338-0190.

Circle No 370

MICROPROCESSOR

The 80186-12 μP is a 12.5-MHz version of the 16-bit 80186 μP. According to the manufacturer, the chip can operate twice as fast as its predecessor. Because it's manufactured with a proprietary 1.5-μm HMOS-III process, it has a 30% smaller die size. The μP combines a CPU with the equivalent of 20 components on one chip and is available in three packages: a PLCC, a pin-grid-array package, and an LCC. You can choose from commercial, industrial, and military grades. \$36 (100). Samples are available now, and production quantities are scheduled for mid-1986.

Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. Phone (408) 496-4580.

Circle No 371

CMOS LOGIC DEVICES

The V54/74 ACT family of CMOS interface logic devices provides 50 interface functions, including 8-, 9-, and 10-bit buffers, latches, flip-flops, and transceivers. Fabricated using a proprietary, 1.6-μm double-level-metal CMOS process, the devices operate over the industrial temperature range (−40 to +85°C) at frequencies to 75 MHz. Constant current drive is 48 mA, typical

propagation delay is 5 nsec, and typical quiescent power consumption is 5 μW. The company guarantees that ESD protection exceeds 2000V. The devices are housed in 20- or 24-pin plastic DIPs. Prices start at $3.25 (100).

VTC Inc, 2401 E 86th St, Bloomington, MN 55420. Phone (612) 851-5000.

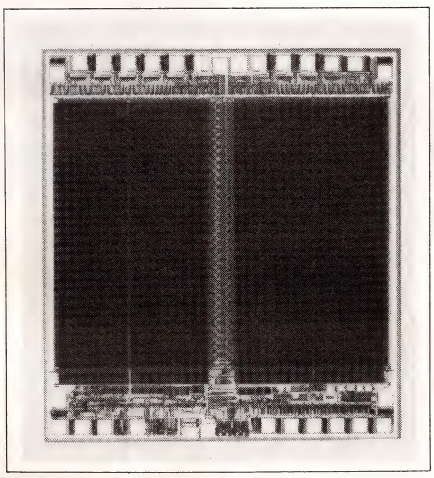
Circle No 372

SMT TRANSISTORS

These 10 bipolar and three TMOS power MOSFETs come in D packs, which the manufacturer claims are the first power packages designed for surface-mount applications. The D pack resembles a miniature TO-220 enclosure and offers cost-reducing features, including the elimination of pc-board through holes, reduction of the size of the pc board, use of both sides of the board, and the ability to handle power levels exceeding 1W. Prices range from $0.54 to $1.53 (100).

Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036. Phone (602) 244-4911.

Circle No 373

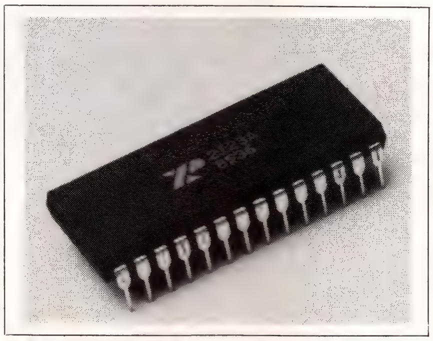


64k-BIT EEPROM

The Am2864B EEPROM features page-mode write and data-bar polling operations and a 250-nsec access time. Data-bar polling on all pins allows a single read-and-comparison operation to determine the chip's status and eliminates the need for external hardware. The 32-byte page-mode operation allows you to write one to 32 bytes of data in one write cycle; according to the manufacturer, the write cycle takes half the time that other 64k-bit EEPROMs require. Organized as 8k×8 bits, the EEPROM has a ready/busy pin that automatically signals the μP that the write cycle is complete. Available in a side-brazed package or a ceramic DIP, $22.27 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 982-7448.

Circle No 374



MODEM IC

The XR-2123A belongs to the phase-shift-keying (PSK) family of devices for full-duplex (to 1200 bps) and half-duplex (to 2400 bps) modem applications. You can program the IC to meet Bell 212A and 202 or CCITT V.22 and V.26 specifications; the device provides the ±7-Hz carrier-capture range required to meet the CCITT standards. If you want the modem to operate asynchronously, you'll need the XR-2125 synchronous-to-asynchronous converter. Phase-locked loops provide digital demodulation functions, and the modulator provides a synthesized sine-wave output in a dibit PSK format. The CMOS IC requires ±5V supplies and operates between 0 and 70°C. It comes in a 28-pin plastic or ceramic DIP. $13.85 (100).

Exar Corp, 750 Palomar Ave, Sunnyvale, CA 94088. Phone (408) 732-7970. TWX 910-339-9233.

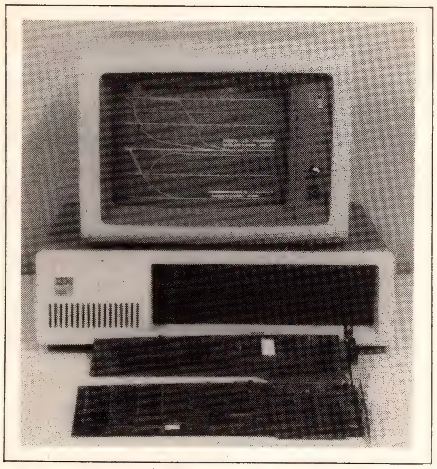
Circle No 375

1986 EDN CARAVAN TRAVELING ELECTRONIC SHOW

February 24 to March 28 (first half)

DATE	TIME	SITE
day	8-9:30 AM	IBM CORPORATION 1000 NW 51st St., Boca Raton, FL
day	10:15-12 AM	IBM CORPORATION 1626 S. Congress Ave., Del Ray, FL
day	1:30-3 PM	MOTOROLA INC. 1500 NW 22nd Ave., Boynton Beach, FL
5 sday	8-9:30 AM	BENDIX AVIONICS 2100 NW 62nd St., Ft. Lauderdale, FL
5 sday	10:30-12 AM	RACAL-MILGO 1601 N. Harrison Parkway, Sunrise, FL
5 sday	2-4:30 PM	MOTOROLA INC. 8000 W. Sunrise Blvd., Plantation, FL
6 nesday	9-12 AM	HARRIS CORPORATION GOVERNMENT SYSTEMS Palm Bay Rd., Palm Bay, FL
6 nesday	2-3:30 PM	HARRIS CORPORATION SATELLITE COMMUNICATIONS 1380 Harris Rd., Melbourne, Fl
7 rsday	8-9:30 AM	MARTIN MARIETTA AEROSPACE E. Sand Lake Rd., Orlando, FL
7 rsday	10:30-12 AM	MARTIN MARIETTA AEROSPACE 12506 Lake Underhill Dr., Orlando, FL
7 rsday	2:30-4:30 PM	GENERAL ELECTRIC CO. 1800 Volusia Ave., Daytona Beach, FL
8 ay	8-9:30 AM	E-SYSTEMS, INC. ECI DIVISION 1501 72nd St. North, St. Petersburg, FL
8 ay	10:30-12 AM	PARADYNE CORPORATION 8550 Ulmerton Rd., Largo, FL
8 ay	2-4:15 PM	HONEYWELL INC. AVIONICS 13350 Hwy 19, Clearwater, FL
nday	8:30-9:45 AM	CHRYSLER MILITARY-PUBLIC ELECTRONIC SYSTEMS 5021 Bradford Dr., Huntsville, AL
nday	10:30-12 AM	CHRYSLER ELECTRONICS DIVISION 102 Wynn Dr., Huntsville, AL
nday	1-2 PM	SCI SYSTEMS, INC. 5000 Technology Dr., Huntsville, AL
3 nday	3-4:30 PM	SCI SYSTEMS, INC. 8600 S. Memorial Pkwy, Huntsville, AL
4 esday	8:30-10 AM	SCIENTIFIC-ATLANTA 4311 Communications Dr., Norcross, GA
4 esday	10:45-12 AM	AT&T TECHNOLOGIES 2000 Northeast Expressway, Norcross, GA
4 esday	2-3 PM	SCIENTIFIC-ATLANTA 3845 Pleasantdale Rd., Doraville, GA
5 ednesday	8:30-9:45 AM	ROCKWELL INTERNATIONAL CORPORATION 1800 Satellite Blvd., Duluth, GA
5 ednesday	10:30-11:30 AM	ROCKWELL INTERNATIONAL CORPORATION Gwinnett Industrial Park, Norcross, GA
6 ursday	9-10:30 AM	NCR CORPORATION 3325 Platt Springs Rd., West Columbia, SC
6 ursday	2-4 PM	IBM CORPORATION 1001 Harris Blvd., Charlotte, NC
7 iday	9-11:30 AM	IBM CORPORATION Research Triangle Park, NC
7 iday	1-2:15 PM	NORTHERN TELECOM INC. BNR Research Triangle Park, NC
7 iday	3-4:15 PM	IBM CORPORATION 2520 North Blvd., Raleigh, NC
/10 onday	8:30-9:30 AM	ITT TELECOMMUNICATIONS 2912 Wake Forest Rd., Raleigh, NC
/10 onday	10:15-11:30 AM	ITT TELECOMMUNICATIONS 3127 Smoketree Ct., Raleigh, NC
/10 onday	1-2 PM	ITT TELECOMMUNICATIONS 6131 Falls of the Neuse Rd., Raleigh, NC

DATE	TIME	SITE
3/10 Monday	3-4:30 PM	TELEX TERMINAL COMMUNICATIONS 3301 Terminal Dr., Raleigh, NC
3:11 Tuesday	8:30-9:45 AM	AT&T TECHNOLOGIES, INC. 204 Graham Hopedale Rd., Burlington, NC
3/11 Tuesday	2:30-4:30 PM	GENERAL ELECTRIC CO. 1501 Roanoke Blvd., Salem, VA
3/12 Wednesday	9-10:30 AM	GENERAL ELECTRIC CO. Mountain View Rd., Lynchburg, VA
3/12 Wednesday	1:30-3:30 PM	GENERAL ELECTRIC CO. U.S. Hwy 29 North, Charlottesville, NC
3/13 Thursday	9-11 AM	IBM CORPORATION 9500 Godwin Dr., Manassas, VA
3/13 Thursday	1-2:45 PM	E-SYSTEMS, INC. MELPAR DIVISION 7700 Arlington Blvd., Falls Church, VA
3/13 Thursday	3:30-4:30 PM	E-SYSTEMS, INC. MELPAR DIVISION 11225 Waples Mill Rd., Fairfax, VA
3/14 Friday	9-11 AM	LITTON SYSTEMS, INC. AMECOM DIVISION 5115 Calvert Rd., College Park, MD
3/14 Friday	1:30-3 PM	WESTINGHOUSE ELECTRIC OCEANIC DIVISION Oceanic Dr., Annapolis, MD
3/17 Monday	8:30-11 AM	WESTINGHOUSE ELECTRIC AESD & CCD Baltimore Int'l Airport, Baltimore, MD
3/17 Monday	1-2:15 PM	BENDIX COMMUNICATIONS DIVISION 1300 E. Joppa Rd., Baltimore, MD
3/17 Monday	3-4:30 PM	AAI CORPORATION York Rd. & Industry Ln., Cockeysville, MD
3/18 Tuesday	9-11:30 AM	RCA CORPORATION Front & Cooper St., Camden, NJ
3/18 Tuesday	1:30-4 PM	RCA CORPORATION Marne Hwy., Moorestown, NJ
3/19 Wednesday	9-12 AM	AT&T BELL LABORATORIES Crawfords Corner Rd., Holmdel, NJ
3/19 Wednesday	2-4 PM	AT&T INFORMATION SYSTEMS 200 Laurel Ave., Middletown, NJ
3/20 Thursday	8:30-9:45 AM	SYSTEMS DEVELOPMENT CORP., A BURROUGHS CO. Swedsford Rd., Paoli, PA
3/20 Thursday	10:30-12 AM	BURROUGHS SDG Swedsford Rd., Paoli, PA
3/20 Thursday	2-4 PM	SPERRY CORPORATION Union & Jolly Rd., Blue Bell, PA
3/21 Friday	9-11 AM	HONEYWELL PROCESS CONTROL DIVISION 1100 Virginia Dr., Ft. Washington, PA
3/21 Friday	1:30-3 PM	RCA CORPORATION 201 Washington Rd., Princeton, NJ
3/24 Monday	9-10:30 AM	AT&T BELL LABORATORIES 555 Union Blvd., Allentown, PA
3/24 Monday	2-4 PM	LOCKHEED ELECTRONICS US Hwy 22, Plainfield, NJ
3/25 Tuesday	9-11 AM	AT&T BELL LABORATORIES 600 Mountain Ave., Murray Hill, NJ
3/25 Tuesday	1:30-4 PM	AT&T BELL LABORATORIES Whippany Rd., Whippany, NJ
3/26 Wednesday	9-11 AM	HEWLETT-PACKARD CO. 150 Green Pond Rd., Rockaway, NJ
3/26 Wednesday	1:30-4 PM	SINGER CO. KEARFOTT DIVISION 150 Totowa Rd., Wayne, NJ
3/27 Thursday	9-11 AM	ITT DEFENSE COMMUNICATIONS 492 River Rd., Nutley, NJ
3/27 Thursday	1-3 PM	ITT AVOINICS 390 Washington Ave., Nutley, NJ



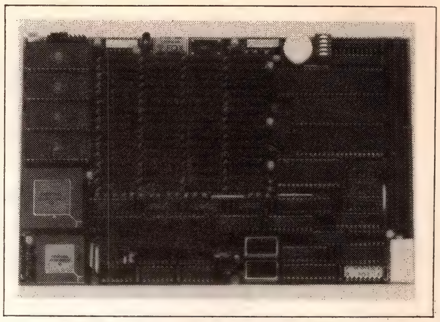
ACQUISITION SYSTEM

The Premas 2-board set plugs into an IBM PC, PC/XT, or PC/AT to sample data from four input channels. It comes with floppy-disk-based support software that directs the hardware to sample the data channels, store the data on the PC's floppy or hard disk, and display a plot on the PC's monitor, all at the same time. By storing data to a disk in real time, the acquisition system can store more data than systems that store only to the PC's memory. Using the software, you program each of the four channels to one of four input ranges—±300 mV, ±3V, ±30V, or ±300V—and to one of three degrees of resolution—12, 16, or 19 bits. Sample rates for the three degrees of resolution are 33, 10, and 2.5 samples/sec, respectively. You can program the board for autozeroing and autoranging modes. $1465.

Dataq Instruments Inc, 100 Lincoln St, Akron, OH 44308. Phone (216) 434-4284.

Circle No 377

SINGLE-BOARD μP

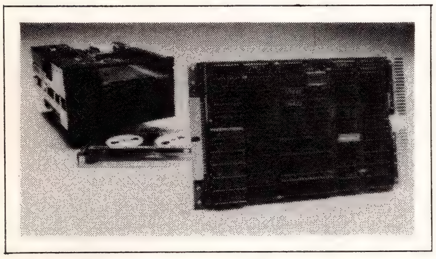


The MC68020 μP powers the Micro-20 single-board computer. The computer includes 2M bytes of RAM, as much as 256k bytes of EPROM, four serial ports, and an 8-bit parallel port. A controller for 5¼-in. floppy disks, an SASI-peripheral interface, and a 16-bit expansion connector attach I/O devices to the computer. The 8.8×5.75-in. board mounts in the same space as a standard 5¼-in. floppy-disk drive, and it uses the same supply voltages as the drive. A separate board, included with the computer, provides RS-232C-level translation and DB-25-type connectors for the serial ports. The computer draws 4.5A from a 5V supply and 125 mA from a 12V supply; it generates its own −12V supply. With 020Bug monitor/debugger and

hardware diagnostics, $2200 (25).

GMX Inc, 1337 W 37th Pl, Chicago, IL 60609. Phone (312) 927-5510. TWX 910-221-4055.

Circle No 378



TAPE CONTROLLER

The STC-TSQ11 emulates Digital Equipment Corp's TK25/TS11 to connect LSI-11 computer systems to QIC-2 streaming-tape cartridge drives. The drives back up large-capacity hard disks, saving or restoring 60M bytes of data on a ¼-in.-tape cartridge in 12 minutes. The controller connects to LSI-11 computers, including the MicroVAX II, and works under operating systems and applications programs that control the TK25/TS11. Its dual-wide Q Bus module fits in a Q Bus backplane slot. $1250.

Sigma Information Systems, 3401 E La Palma Ave, Anaheim, CA 92806. Phone (714) 630-6553. TLX 298607.

Circle No 379

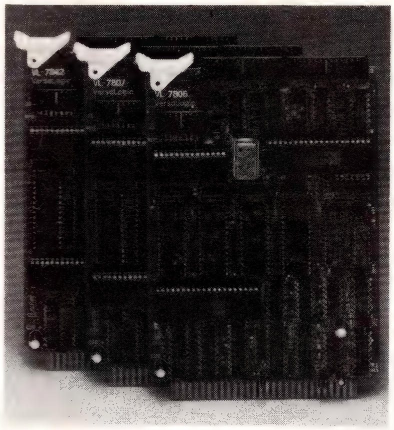
MS-DOS ON STD BUS

You can run programs developed under MS-DOS on the STD Bus by adding either the STD-DOS prototyping system (PS 1.1) or the STD-DOS OEM system (OS 1.1) to the STD Bus. Both systems plug into the STD Bus and connect to IBM PC-compatible computers through an RS-232C link. You can develop programs for the STD Bus on the PC and then download them to the systems. Both systems include MS-DOS 3.1 in ROM, support utilities on floppy disks, and 8088-based CPU cards. The PS 1.1 also offers four memory cards, an extender card, a card cage, a power supply, and the RS-232C cable. $2895. The OS 1.1 has only the CPU, two memory cards, and utility disks, but it can run applications developed on the PS 1.1. $1690.

Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940. Phone (408) 372-4593. TWX 910-360-7082.

Circle No 380

CIRCLE NO 113



STD BUS BOARDS

STD Bus-compatible single-board computers in the VL-7800 Series, which are plug-in replacements for Pro-Log's Z80-based models, are available in 6-MHz versions. The series comprises three processor boards, each of which is available in 2.5-, 3.68-, 4-, and 6-MHz versions. The VL-7806 has two RS-232C channels; the VL-7807 provides one RS-232C channel and one 8-bit Centronics port. The VL-7842 version offers either two RS-422 channels or one RS-422 and one RS-232C channel. All three boards use a buffered Z80 CPU and include sockets for as much as 128k bytes of onboard RAM or EPROM; three general-purpose, 8-bit counter/timers; and vectored interrupt inputs. C4 Basic for industrial-control applications and the companion Novos (nonvolatile operating system) permit program storage in nonvolatile IC memory. The boards carry a 3-year warranty. 6-MHz versions, $300 to $330.

VersaLogic Corp, 87070 Dukhobar Rd, Eugene, OR 97402. Phone (800) 824-3163; in OR, (503) 485-8575.

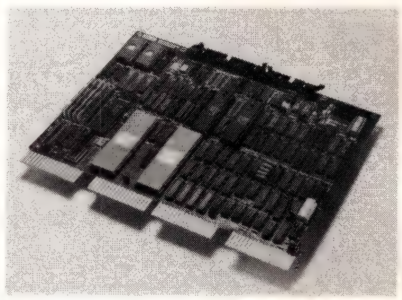
Circle No 381

1-BOARD COMPUTER

The Cobra/16 single-board computer is based on the DEC J11 16-bit CPU chip. The module includes a 15-MHz CPU with floating-point arithmetic, a 4k-byte bipolar cache memory, 512k bytes of dynamic RAM, 5¼-in. ST506 Winchester disk and SA850 floppy-disk controllers, and a 4-port serial interface. The board measures 11.5×12 in. and supports PDP-11-compatible operating systems, including RSX11/M, RSX11/M-Plus, RT11, RSTS/E, TSX-Plus, Mumps, and Unix. It's available as a board-level product, in a desktop chassis, or in a custom system. Less than $3000.

General Robotics Corp, 57 N Main St, Hartford, WI 53027. Phone (414) 673-6800. TLX 269686.

Circle No 382

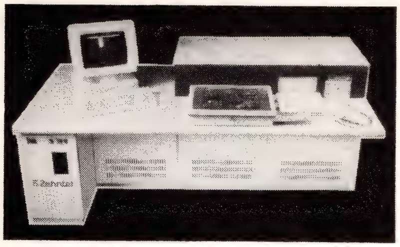


X.25 INTERFACE

The 5250 single-board MicroVAX front-end communications processor with onboard X.25 firmware allows users of MicroVAX II and other Q Bus computers to connect to packet-switched networks, including Telenet, Tymnet, and DDN. Two versions are available: The Basic Mode comes with 128k bytes of memory and standard network default capacities. The Extended Mode provides 512k bytes of memory, frame and packet sizes of 1024 bytes, and extended sequence numbering. Both versions accommodate as many as 128 switched or permanent circuits at network-line speeds as fast as 64k bps. Basic Mode, $5290; Extended Mode, $5890.

Advanced Computer Communications, 720 Santa Barbara St, Santa Barbara, CA 93101. Phone (805) 963-9431. TWX 910-334-4907.

Circle No 383

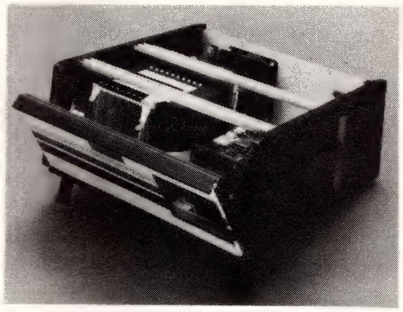


32-BIT BUS ATE

The Z3200 tester for boards with 32-bit buses includes a performance-test unit, which comprises two bus-timing emulators and which is synchronized with a functional-test unit. The tester features diagnostics via a guided probe. Bus-structured boards with or without µPs can be tested at full speed, with bus-cycle and pattern bursts to 12 MHz. Timing-interface pods are available for boards based on 80186, 80286, 68000, and 68020 µPs. In combination with the programmable bus pod, the tester can emulate Multibus or VME Bus boards. A measurement module provides CRC readings to 40 MHz and frequency measurements to 100 MHz. $250,000.

Zehntel Automation Systems, 2625 Shadelands Dr, Walnut Creek, CA 94598. Phone (415) 932-6900.

Circle No 384



STD BUS DEVELOPER

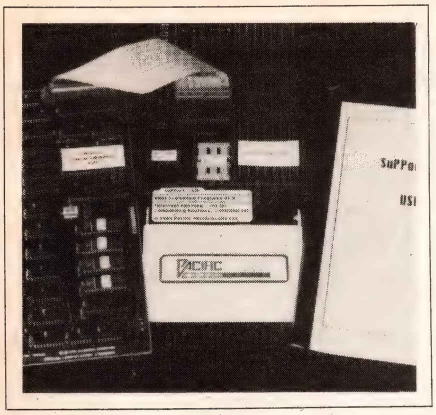
The Over-Nighter, a portable version of the company's Z80-based STD Bus development system, contains an 8-slot card cage, a 75W switching power supply, a fan, two floppy-disk drives, and STD Bus cards for a CP/M development computer. The unit measures 17×17×7 in. and fits a 19-in. rack. Options include additional mounting rails, EPROM programmers, terminals, printers, and development software as well as 10-, 12-, and 16-slot card cages and a 10M- or 20M-byte hard-disk drive. A 4-MHz, Z80-based configuration with 64k bytes of static RAM, an 8-slot card cage and power supply, two card-mounted microfloppy-disk drives, and CP/M operating system costs $2790.

Computer Dynamics Inc, 105 S Main St, Greer, SC 29651. Phone (803) 877-7471.

Circle No 385

DEVELOPMENT BOARD

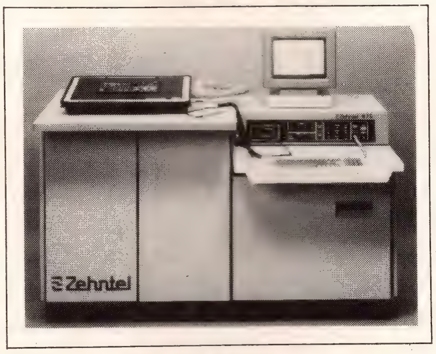
With the Support 329 DB01 development board, you can evaluate the company's PD32HC01, an interface



IC for Texas Instruments' TMS 32010 digital-signal-processor chips. The board allows you to access the PD32HC01 using TI's EVM module or XDS development system. The interface IC provides a serial codec interface, an RS-232C port, I/O and interrupt control, an I/O expansion interface, and a 2400-Hz bit-rate generator. The board also includes a μlaw Codec, RAM and ROM, a 32010 socket, and an uncommitted breadboarding area for prototyping additional functions. $475.

Pacific Microcircuits Ltd, Product Development Group, 240 H St, Blaine, WA 98230. Phone (604) 536-1886.

Circle No 386



IN-CIRCUIT ATE

The Model 875 in-circuit tester can have as many as 640 hybrid, non-multiplexed test points. The tester runs the same software and accepts the same test programs as other devices in the 800 Series. The tester can have as many as 512 digital test points plus analog test points backed by a 16-bit A/D converter. The unit incorporates a 68010-based computer and runs the Unix operating system. An operator-training package is included. The Model 875 with 208 test points costs less than $85,000.

Zehntel Automation Systems, Box 8016, Walnut Creek, CA 94596. Phone (415) 932-6900. TLX 3716185.

Circle No 387

600W SWITCHER

The Case 22/23 switching power supply delivers 300 to 600W from as many as seven outputs. The supply measures 3×5×14.25 in. and meets UL, CSA, IEC, and VDE certification requirements. Load regulation is 1% for all outputs having remote sensing or 2% for outputs without remote sensing. Line regulation is 1%±15% of line-voltage range. The

supply has a built-in fan. Less than \$1/W (100). Delivery, six to eight weeks ARO.

Qualidyne Systems Inc, 3055 Del Sol Blvd, San Diego, CA 92153. Phone (619) 575-1100.

Circle No 388

IN-CIRCUIT EMULATOR

Unlike other small emulators, the Icebox has 65,535 true hardware breakpoints and performs full-speed emulation. It maintains the Z80 and NSC800 refresh signals during all phases of operation, so that dynamic memories in the target system will retain their data. The emulator uses the target system's V_{CC} to operate, requiring less than 500 mA. If the target system doesn't have enough available power, you can use an external power source. The emulator is available for the Z80, 8085, and NSC800 processors. \$600.

Softaid Inc, Box 2412, Columbia, MD 21045. Phone (301) 792-8096.

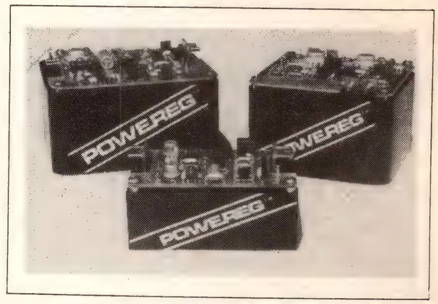
Circle No 389

GRAPHIC CALCULATOR

At the touch of a button, the FX7000G scientific calculator lets you make graphic representations of numerical equations. Furthermore, the calculator displays changes in numerical values as continuous graphic fluctuations. You can simultaneously portray two or more function equations in one graphic display or mix several equations as a combined graph. The FX7000G also displays the intersection and approach of different functions, maximum and minimum points, and other mathematical characteristics. The calculator has a 2.17×1.5-in. LCD with a resolution of 96×64 dots. The unit weighs about 5.5 oz and measures 3.3×6.5×0.5 in. \$99.95.

Casio Inc, 15 Gardner Rd, Fairfield, NJ 07006. Phone (201) 575-7400.

Circle No 390



MIL SUPPLIES

Military power supplies in the Powereg Series provide as many as five outputs, output voltage ranges of 2 to 28V dc, and output current ranges from 2 to 70A. The supplies operate over −55 to +85°C (baseplate temperature) and meet MIL-STD 202 (Method 204D, condition D and Method 214, condition J) requirements for vibration. A multiple-output converter has a 2-transistor forward-converter module and a saturable-reactor regulator module for each output. The module meets DOD-STD-1399 and MIL-STD-704D and -461B, Part 4 CE03; it features current limiting, undervoltage lockout, and inrush-current limiting. MTBF, under Navy-sheltered conditions and per MIL-HDBK-217D, is over 90,000 hours. Line and load regulation are 1.0%. Additional features include a 2-stage filter for low noise operation and optional status indicators. \$12.50 to \$20/W. Delivery, 10 weeks ARO.

ATC Power Systems Inc, 472 Amherst St, Nashua, NH 03063. Phone (603) 882-1366. TLX 756779.

Circle No 391

GATE ARRAYS

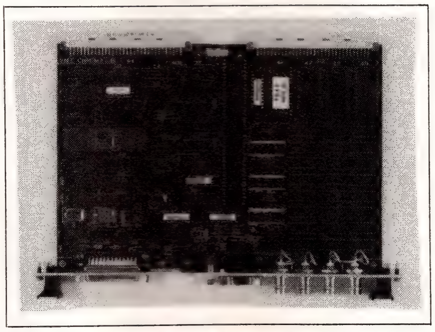
Providing respective gate counts of 3289, 4290, and 6000, the M3000C2, M4000C2, and M6000C2 2-μm double-metal-layer gate arrays feature a 2-input NAND gate propagation delay of 1.7 nsec and a toggle frequency of 100 MHz max. I/O pin counts are 90, 104, and 130, respectively; you can use the TTL- and CMOS-compatible I/O buffers as standard- or Schmitt-trigger inputs and as push-pull or drain-driver outputs. The manufacturer offers a library of more than 60 macrocells, including gates, flip-flops, and I/O buffers, and a library of 38 soft macrocells. The gate arrays are available in commercial, industrial, and military grades in ceramic or plastic DIPs as well as ceramic or plastic pin-grid-array and PLCC packages. PLCC gate arrays, approximately Fr fr 130 (M3000C2) to Fr fr 350 (M6000C2) (10,000).

Thomson Semiconductors, 43-45 Ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 240780.

Circle No 392

Thomson-CSF Components Corp, Semiconductor Div, 301 Rte 17 N, Rutherford, NJ 07070. Phone (201) 438-2300.

Circle No 393



GRAPHICS CARD

Providing interlaced 512×512-pixel resolution and 8-color display, the PG3200 color-graphics display module operates in a VME Bus or stand-alone environment. Based on an EF9365 graphic-display processor and a 68121 intelligent peripheral controller, the module interfaces with raster-scan RGB monitors. Onboard memory accommodates two screen pages, and the dual-ported RAM is accessible via the VME Bus or the 68121. An RS-232C interface handles stand-alone operation. Onboard firmware is provided for point and vector plotting, variable-size ASCII-character generation, and the display of circles. A light pen is optional, and provision is made for image read-back and read-modify-write operations. $1595.

Philips, Industrial & Electro-acoustic Systems Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 394

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 739-7700.

Circle No 395

INTERNATIONAL

DATACOMM IC

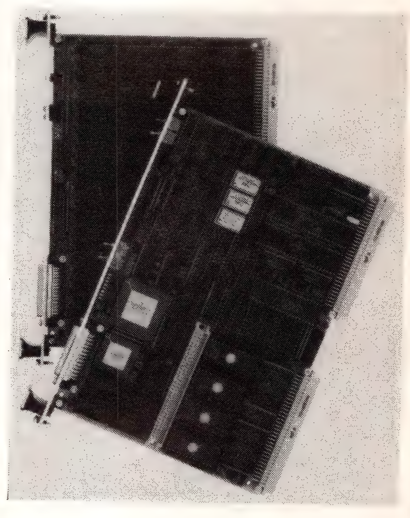
Combining a direct-memory-access (DMA) and a high-level data-link controller (HDLC) in one package, the MV6001EXP relieves CPU resources of the overhead involved in handling data links. To transmit or receive a block of data, the processor specifies the start address and length of the data block in memory; the device then handles the block transfer and formatting without further processor intervention. It operates at DMA rates as high as 8 MHz; HDLC frame lengths are programmable to 2k bytes. The device automatically appends a frame-check sequence. £20.46 (1000).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wilts SN2 2QW, UK. Phone (0793) 36251. TLX 449637.

Circle No 396

Plessey Solid State, 3 Whatney Ave, Irvine, CA 92718. Phone (714) 951-5212.

Circle No 397



32-BIT CPU CARDS

The SYS68K/CPU-20/21 CPU modules for VME Bus systems run 16.7-MHz 68020 μPs with no-wait-state access via the FLME Bus (Force Local Memory Extension Bus) to 512k bytes of static RAM, which is housed on an accompanying SYS68K/SRAM-22 board. The only

difference between the CPU-20 and the CPU-21 is that the latter contains a 68881 floating-point coprocessor; the CPU-20 has a socket for that coprocessor. Each CPU card features eight sockets for as much as 512k bytes of EPROM or 128k bytes of static RAM, one RS-232C and one RS-232C/RS-422 serial I/O port, interrupt control, and timer functions. The board's VME Bus interface is capable of 32-bit addressing and 32-bit data transfers; it includes a 7-level interrupt handler, single-level bus arbiter, and software-programmable bus-release functions. In addition to the FLME Bus, the board also has a VMX Bus interface. Firmware supplied with the board includes a debug monitor and line assembler/disassembler. The CPU-20 and CPU-21, including the 512k-byte RAM card, cost DM 16,590 and DM 17,565, respectively.

Force Computers GmbH, Daimierstrasse 9, 8012 Ottobrunn, Munich, West Germany. Phone (089) 6092033. TLX 524190.

Circle No 398

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

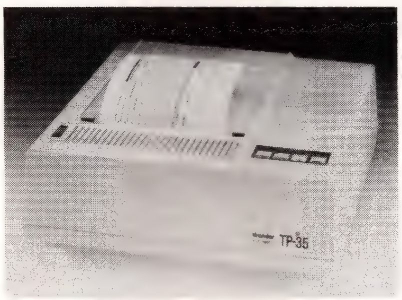
Circle No 399

SEMICUSTOM SUPPLIES

System-Eureka semicustom power supplies are configured from standard chassis, line-input RFI filters, toroidal power transformers, and low-voltage linear or switch-mode secondary regulator modules. These modular components meet safety and emission requirements of agencies such as UL, CSA, and VDE. The RFI filter modules conform to VDE 0871B and FCC 20780B and may be fitted with listed line input components such as the line cord connector, input voltage selector, and fuse and power switches. The toroidal power transformers, listed under UL and VDE, are available with ratings of 80, 160 and 250 VA. Switch-mode secondary regulators are available with output voltages of 5, 12, or 15V at 4A, or with an output voltage of 24V at 3A. Linear regulator modules are available for the same voltages, with either one or two isolated outputs. Switch-mode regulator modules feature current-limit adjustment, provision for switching frequency synchronization, and a power-fail status output. Both switch-mode and linear types have crowbar-overvoltage, thermal overload, and short-circuit protection. Standard chassis assemblies accept two, three, or four regulator packages. The dimensions of a 3-regulator chassis are 4.75×12.5×2 in. A typical 3-module, 4-output power supply, including the RFI filter and line connector, is priced at around $1.50 per watt (OEM qty).

Ulveco Power Products AB, Box 43, S-18400 Akersberga, Sweden. Phone (0764) 66060. TLX 13514.

Circle No 400



VIDEO PRINTER

The TP35 video printer with thermal print head produces graphic and text CRT images from composite video-input signals, separate video signals, or composite sync signals. It can print either positive or negative images on a 6-dot/mm print pitch and operates in either a high- or low-resolution mode. £1085.

Thandar Electronics Ltd, London Rd, St Ives, Huntingdon, Cambs PE17 4HJ, UK. Phone (0480) 64646. TLX 32250.

Circle No 401

80286 ASSEMBLER

Macro Assembler 4.0 runs under MS-DOS on computers that use the 80186, 80286, 80287, 8086, 8087, and 8088 instruction sets. The assembler comes with an interactive source-level symbolic debugger, a linker, a program-maintenance utility, a library manager, a cross-reference utility, and EXE file-packing and header utilities. The 4.0 version allows you to assemble larger source files with more symbols and more macrotext than previous versions; additional assembly switches are also included. Screen swapping permits switching between the debugging screen and the application output. The company claims the assembler provides 100% source- and object-code compatibility with earlier versions of its and IBM's macroassemblers. The package requires 128k bytes of RAM, MS-DOS 2.0 or higher, and one floppy-disk drive, although two drives are recommended. $150; upgrade for registered owners, $75.

Microsoft Corp, Box 97200, Bellevue, WA 98009. Phone (800) 426-9400; in WA, (206) 828-8080. TLX 328945.

Circle No 402

PARALLEL ADA

VADS, a parallel implementation of the Ada development system, runs on Sequent's (Beaverton, OR) Balance 8000 parallel computer. According to the company, the multistream nature of Ada development and execution allows the package to use the tightly coupled, parallel architecture of the Balance system for reduced development time and higher run-time performance. The package provides an Ada compiler and a set of software-development tools, which includes an interactive screen-oriented debugger, library-management tools, and the run-time system. Prices start at $15,000 for a 16-user system.

Verdix Corp, 14130-A Sullyfield Circle, Chantilly, VA 22021. Phone (703) 378-7600.

Circle No 403

VOICE RECOGNITION

With VoiceCommand and an IBM PC, PC/XT, or PC/AT, you can operate such programs as Lotus 1-2-3 and Wordstar by voice; the personal computer accepts voice commands as it would commands entered via a keyboard. Users define such common commands as "create graph," "initialize program," and "save data," which are stored for use with other software packages. The system has space for a 500-word vocabulary, but you can overlay multiple 500-word segments for a total of 8000 words. A voice-defined menu option can replace standard soft-

ware menus; you can link menus to form a complete voice system. The package includes the software, a microphone, a plug-in board, and an instruction manual. $399.

Interpath Corp, 3333 Bowers Ave, Suite 253, Santa Clara, CA 95054. Phone (408) 988-3832.

Circle No 404

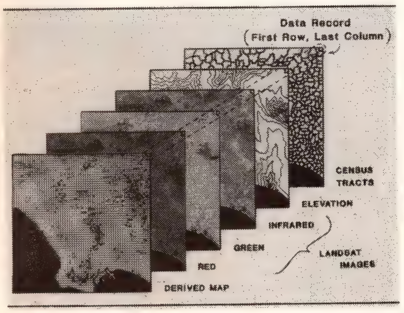


IMAGE PROCESSING

PICDMS, a database-management system for image processing and model building, operates in two or more dimensions on digitized photographs, maps, and drawings. It can detect objects or edges in pictures, recognize and classify patterns, determine minimum and maximum values, calculate distances, and create histograms and statistical analyses. The software runs on Prime minicomputers, Apple II, and the IBM PC and compatibles. A 1-time license fee for microcomputer version, $5000; minicomputer version, $8000.

MIB Chock, 1048 24th St, Santa Monica, CA 90403. Phone (213) 828-4788.

Circle No 405

DATABASE SYSTEM

This company's relational database-management system is available in an MS-DOS version. The package provides a comprehensive set of development tools, including SQL and fourth-generation report writer. The package is upward compatible with Unix. A host-language interface to the C language allows you to integrate existing or custom subroutines into your applications. Without the host-language interface, $995; host-language interface, $495.

Unify Corp, 4000 Kruse Way Pl, Lake Oswego, OR 97034. Phone (503) 635-6265. TLX 469220.

Circle No 406

MS-DOS LINK

The L/F-Link interface program allows the single-user MS-DOS operating system to function under the supervision of the multiuser TurboDOS operating system. The program and the company's S-100+ Bus permit direct user-to-file-server communications and virtually eliminate bus contention. TurboDOS is a multiprocessor operating system that can coordinate a network of 80186 processors running at speeds as high as 8 MHz. $495.

L/F Technologies, 2800 Lockheed Way, Carson City, NV 89701. Phone (702) 883-7611. TWX 910-395-6051.

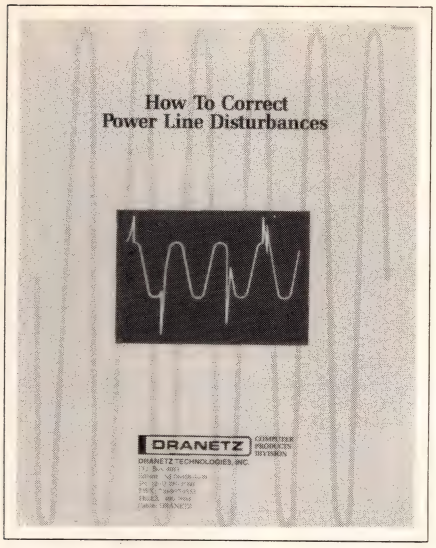
Circle No 407

INVENTORY SYSTEM

The Stock-Master 4.0 inventory-management system runs on the IBM PC, PC/XT, PC/AT, and compatible computers. The 143-program system is organized into eight subsystems that provide master-file maintenance, 12 types of transaction entry and editing, stock status reporting, transaction history detail analysis, trend analysis, purchase-order tracking, quality-control reporting, and system-maintenance utilities. The system has an 18-character part number with two 30-character description fields. It also maintains a record of inventory balances. Object-code license fee, $995.

Applied Micro Business Systems Inc, 177-F Riverside Ave, Newport Beach, CA 92663. Phone (714) 759-0582.

Circle No 408

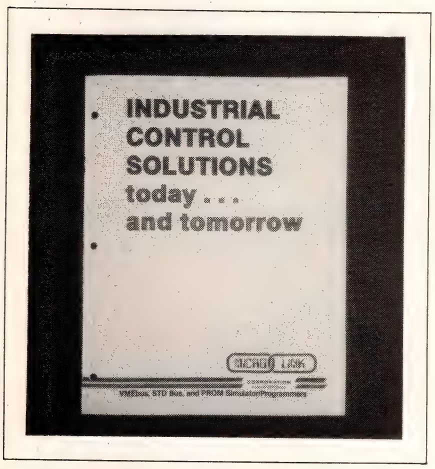


Guide features power-line protection devices

How To Correct Power Line Disturbances is a 16-pg booklet on devices that you can use to protect power lines. It contains descriptions of typical isolation transformers, line voltage regulators, line conditioners, motor-generator sets, and uninterruptible power supplies. A guide to determining the economical justification of protective devices is included.

Dranetz Technologies Inc, Box 4019, Edison, NJ 08818.

Circle No 409



Bus products described

Containing short descriptions of more than 60 STD Bus and VME Bus μC boards, this industrial-control products catalog also covers support software, firmware, and hardware. The products, based on the Z80, 8085, 68000, and 68008 μPs, include single-board computers, CPUs, memory devices, and I/O and communications devices. Also covered is the manufacturer's family of EPROM emulator/programmers. You can use the products in process- and industrial-control applications, ATE, and data-acquisition systems.

Micro-Link Corp, 14602 N US Hwy 31, Carmel, IN 46032.

Circle No 410

DMOS design-contest winners presented

Featuring the winning entries from a double-diffused MOS (DMOS) design contest conducted by the manufacturer, this 60-pg booklet includes a variety of p-channel DMOS products. Also included are DMOS application articles and information on data-sheet interpretation. The publication also contains a cross-reference and product-selection guide.

Supertex Inc, Customer Service Dept, Box 3607, Sunnyvale, CA 94088.

Circle No 411

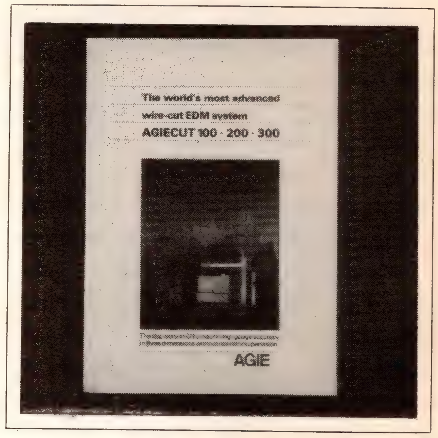
Catalog helps you choose circuit-board indicator

An 8-pg LED circuit-board-indicator catalog lists the company's line of LEDs, which require no lead bending or trimming. The short-

form catalog includes dimensional drawings as well as pertinent specifications so you can choose the proper LED circuit-board indicator. The catalog also lists the company's representatives.

Dialight Corp, 203 Harrison Pl, Brooklyn, NY 11237.

Circle No 412



Electrical-discharge machines detailed

A series of wire-cut electrical discharge machines (EDM) is the subject of this 4-color, 24-pg brochure. The booklet describes how, via computer control, you can program the Agiecut machine to operate for as long as 60 hours to produce an extrusion die, a progressive die, a copper electrode, six brass template cams, and six carbide punches. The document also provides details of the machine—eg, its cutting speed and contouring capabilities.

Agietron Corp, Box 469, Addison, IL 60101.

Circle No 413

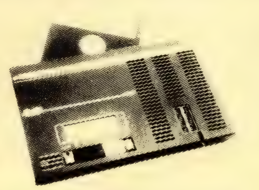
EDN PRODUCT MART

This advertising is for new and current products.

Please circle Reader Service number
for additional information from manufacturers.

MODEL IQ-160 FROM DIGITAL MEDIA

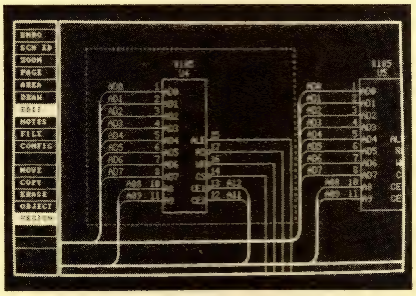
POWERFUL AND INTELLIGENT, FIRST TRULY PORTABLE UNIVERSAL PROGRAMMER



- Programs PAL, PLE, IFL, PROM, EPROM, EEPROM including MOS, CMOS, NMOS, ECL, BI-POLAR
- No personality modules
- Emulates 32K x 8 EPROM/PROM
- Software updatible for new devices
- RS-232 with automatic Baud rate adjust between 300 and 19,200 Baud
- Supports JEDEC and Intex Hex formats
- Built-in ultra fast logic interpreter DMLI
- Built-in data manipulation commands
- Fast/intelligent algorithms for EPROMs
- Can drive automatic handlers and GA-160 Gang Adapter
- DMatic mode eliminates operator caused errors
- Automatic detection of reversed or wrong devices
- Automatic self-calibration
- Stand-alone operation for field service
- Lightweight (2.5 lb.) and portable (10 x 6 x 0.7 inches)
- 32 character LCD display
- Part numbers and operating modes selected from menus
- Tested by MMI, TI and National Semiconductor

Digital Media, Inc. • 3178 Gibraltar Avenue • Costa Mesa • CA 92626 • USA
(714) 751-1373

CIRCLE NO 138

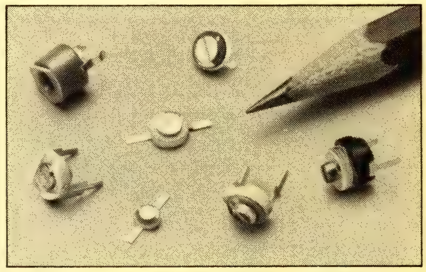


FREE DEMO DISK

SCHEMA is a complete, integrated schematic drawing software package for IBM Personal Computers. Use **SCHEMA** with your PC to draw schematics and automatically generate design documentation such as Wire and Net Lists, Bills of Materials, Design Rule Checks, etc. **SCHEMA** is $495 and supports most common PC hardware configurations. Call or write today for a *free* demo disk and brochure.

OMATION INC.
1701 N. Greenville Ave., Suite 809
Richardson, TX 75081
(214) 231-5167

CIRCLE NO 139



Sprague-Goodman.
The world's largest selection of 5mm (or smaller) trimmer capacitors.

The most wanted features found in various models include high stability, low cost, very small size, and very high Q at high frequency.

Sprague-Goodman Electronics, Inc.

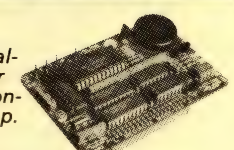
SPRAGUE GOODMAN

(An affiliate of the Sprague Electric Company)
134 Fulton Ave., Garden City Park, NY 11040
516-746-1385 • TLX: 14-4533

CIRCLE NO 140

MULTIBUS:
Your Time Has Come!

The mSBX-241™ Multimodule is a robust, precision Real-Time Clock/Calendar in SBX format with on-board battery backup.



General Features:

- ☐ For high performance systems: no wait states or software overhead
- ☐ Attaches to all SBX and BLX compatible Multibus boards
- ☐ Programmable alarm clock and periodic interrupts
- ☐ 12 or 24 hour time modes, in both BCD and binary format
- ☐ Internal 100 year calendar with leap year compensation
- ☐ Selectable automatic Daylight Savings compensation
- ☐ Contains fifty bytes of general purpose non-volatile RAM
- ☐ **RMX-86/286 drivers supplied on diskette**

For more information contact:

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Intelligent Systems Group
244 West Court, Palatine, Illinois 60067
Telephone (312) 934-4700

Multibus, Multimodule TM Intel Corp.

CIRCLE NO 141

Yours FREE
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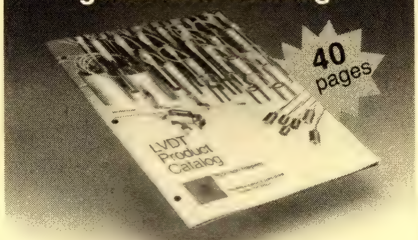

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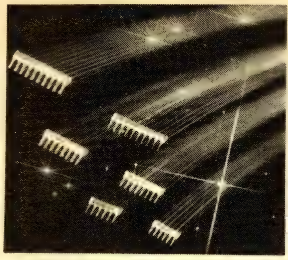

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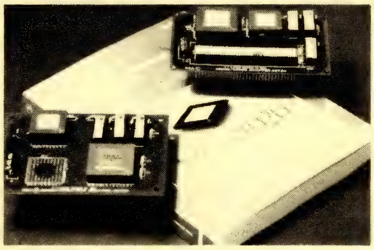

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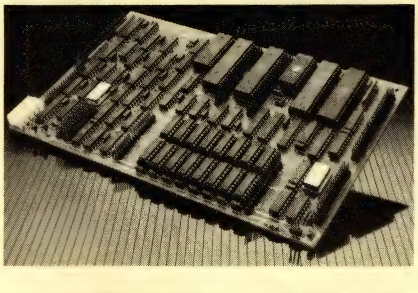

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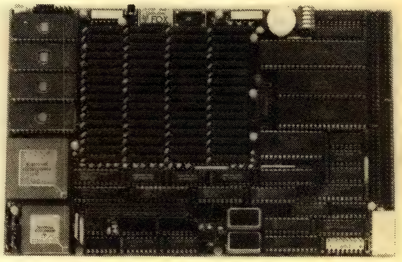

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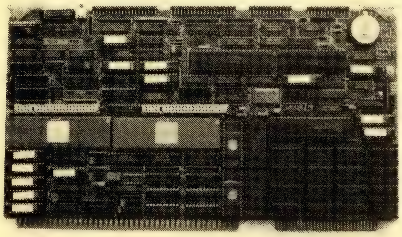

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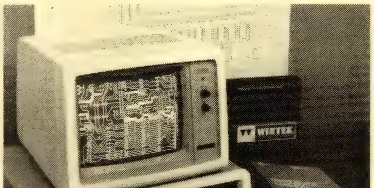

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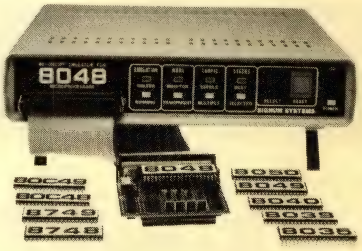

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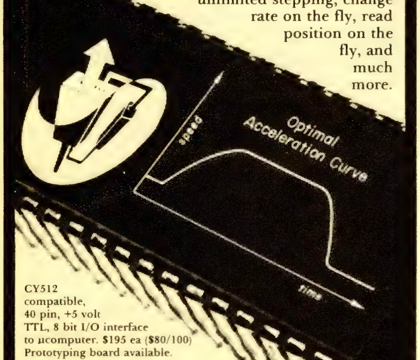

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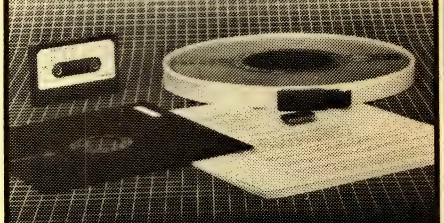

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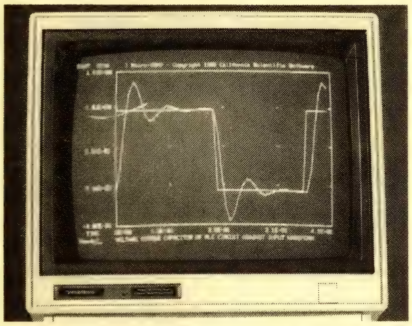

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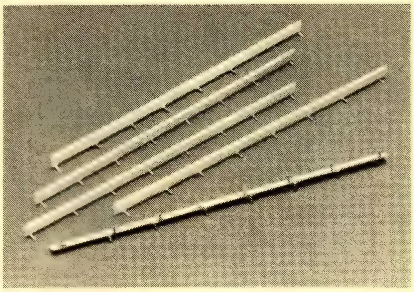

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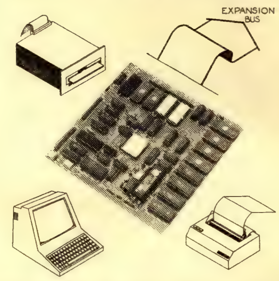

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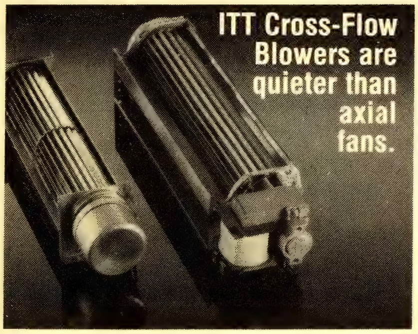

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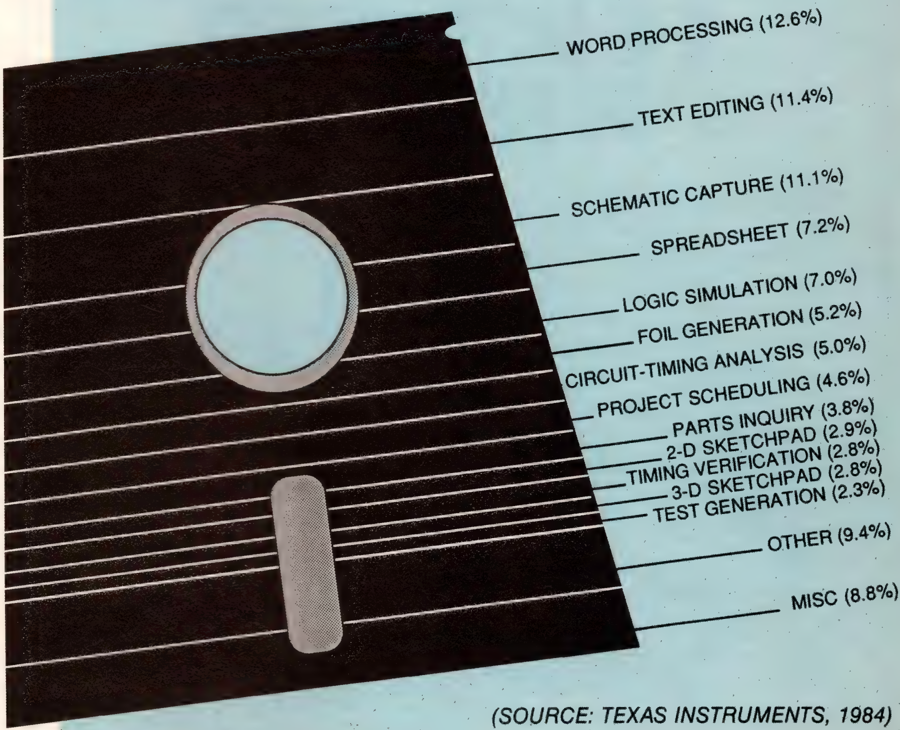
Word-processing software, not a CAE package, is an engineer's most valued assistant

Deborah Asbrand, *Staff Editor*

A study of how engineers at one electronics company put personal computers and software programs to use found that, although engineers were using computer-aided engineering programs for schematic capture, logic simulation, circuit-timing analysis, and functional and behavioral simulation, the programs they used most often were word processing and text editing.

As part of an effort to better assess engineers' computer needs, Texas Instruments launched a survey in 1983, asking its engineers how they spent their time, which tasks they most often performed on computers, and what kind of workstation and software packages they would find useful in their work. Topping the list of useful software programs—ahead of advanced engineering tasks such as schematic capture and logic simulation—was word processing.



A second survey, conducted in 1984, also asked engineers to rank software packages according to how useful they found them in their work. Word-processing and text-editing packages were ranked most useful by the largest number of respondents: 24%. Schematic-capture packages were listed as most important by 11.1% of the respondents; spreadsheets, by 7.2%; logic simulation, by 7%; foil generation, by 5.2%; and circuit-timing analysis, by 5%. Other functions rated important by fewer than 5% of the respondents were project scheduling, functional and behavioral simulation, timing verification, and test generation.

Three hundred engineers at the company's Houston, Austin, and Temple, TX, facilities participated in the two surveys. Forty-four percent of the participants were electrical engineers, most of whom worked in digital, analog, and system design. The bulk of the other participants were mechanical engineers, IC designers, software engineers, and project managers.

Engineers' perceptions of how computers could assist them in their work changed in the year that elapsed between the first and second surveys. Spreadsheets, for example, rose to among the top five packages in the second study, after ranking seventh just one year earlier. Similarly, a higher percentage of engineers rated schematic-capture programs important as compared with respondents in the first survey.

The surveys were actually part of a larger effort by TI's Data Systems Group to develop a strategy for making CAE techniques, then used by a few individuals, available to the group's entire engineering staff. Dick Shaw, manager for engineering services at Texas Instruments' Austin, TX, facility and project manager for the study, says that "a patchwork of stand-alone developments" was occurring throughout the division. One of the project's goals was "to bridge these islands of automation," according to the sur-

vey report, and integrate the use of CAE.

Before the survey was conducted, groups of engineers met first to identify ways in which they could improve their performance and then to determine how CAE programs might help engineers meet those performance goals. The groups identified three top areas for potential improvement: cutting product development time, improving product quality, and enhancing their own productivity.

Shaw says that the results of the surveys at first surprised him and his colleagues. "But as we checked other surveys, they began to make more sense," he recalls. Engineers' tasks involve writing hardware specifications, memos, and reports, Shaw says—all functions that word processing facilitates.

The survey results prove to Shaw that the personal computer is an adequate tool for many engineering applications. "You don't need a big computer to do word processing, foil generation, and schematic capture," he says. A personal computer can handle most of the applications that the engineers listed as most important to them in their work, Shaw claims. As a result, rather than purchase high-end computers, the company makes its personal computer available to engineers. Almost all of the engineers at Texas Instruments are now using personal computers, according to Shaw.

An evaluation process of engineering tools, begun during the study project, has continued at the three TI facilities. After the project's final report was completed last June, approximately 30 participating engineers split up into smaller teams to continue evaluating some of the hardware and software they use. **EDN**

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Mar. 20	Feb.21	Test & Measurement; Analog ICs; Computer Peripherals; Support Chip Directory	Mailing: 3/25
Apr. 3	Mar. 7	Communications Special Issue; Communications ICs; CAE; Buses; April Fools Supplement	Closing: 4/10 Mailing: 4/22
Apr. 17	Mar. 21	Power Supplies; Development Software; Memory Technology; Computer Graphics Devices (CAE-related*); Electro '86 Product Preview	
May 1	Apr. 4	Electro '86 Show Issue; Sensors/Transducers; ICs; Test & Measurement; Display Technology	Closing: 5/8 Mailing: 5/20
May 15	Apr. 18	Programmable Logic Devices; CAE; Communications Components; Optoelectronics	
May 29	May 2	Analog Technology Special Issue; Data Converters; Analog ICs	
June 12	May 16	Digital Technology Special Issue; Personal Computer Boards; Development Systems (CAE-related*); Computer ICs; NCC Show Preview	Closing: 6/19 Mailing: 6/30

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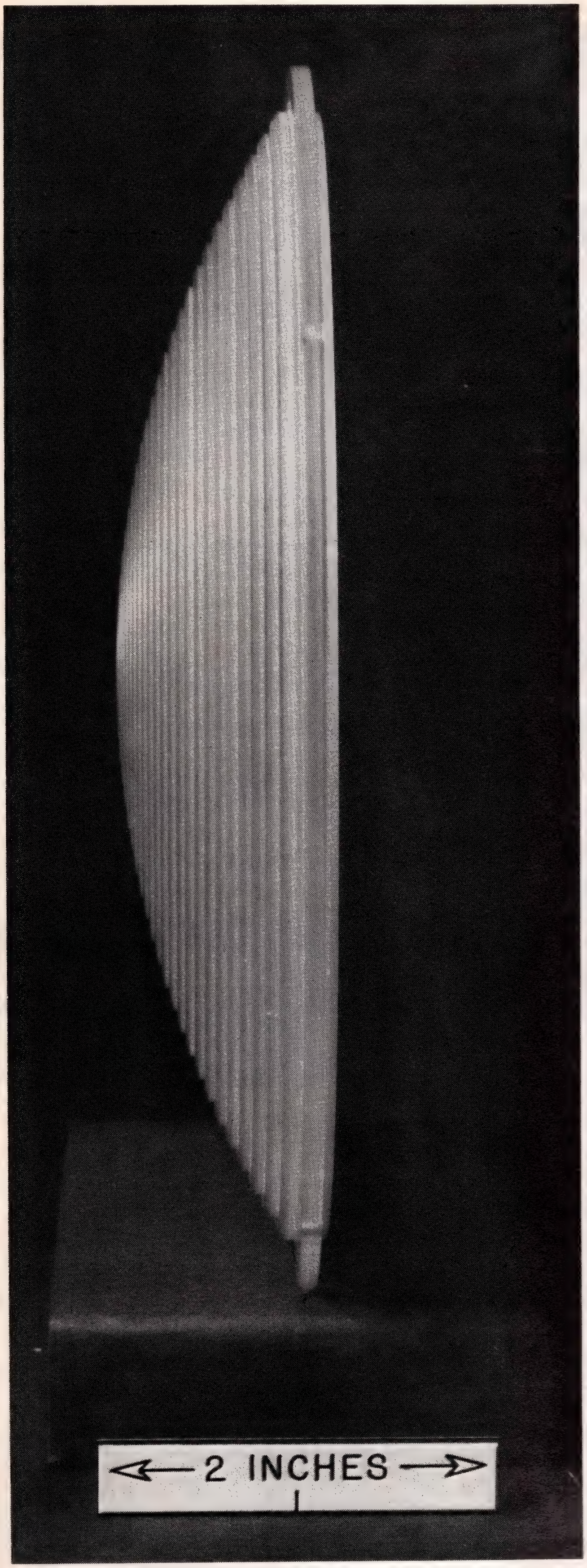
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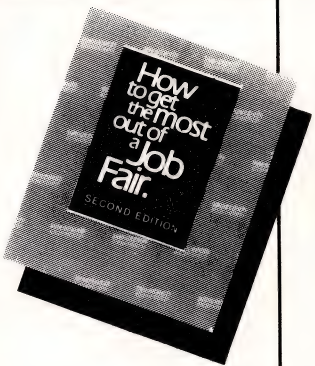

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LOOKING AHEAD

EDITED BY GEORGE STUBBS

1990 connector market to top $7.5 billion

Though final figures for the 1985 connector and IC-socket market are expected to show a decrease in production value of 1.4% compared with the 1984 value, production of the devices (measured in terms of their dollar worth) will grow at an average annual rate of 11.4% throughout the remainder of the decade, according to the market-research company Gnostic Concepts Inc (San Mateo, CA). The production value of connectors and IC sockets was $3.9 billion in 1984; the figure in 1990 should be more than $7.5 billion.

Gnostic Concepts attributes the 1985 decline to inventory surplus accumulated in 1984 and depleted throughout the following year. Growth in production should reach a high point in 1988 (19.9%) and a low point in 1989 (2.4%). The latter growth figure assumes a general economic recession for 1989, as predicted by Data Resources Inc (Lexington, MA).

In keeping with the high growth potential of fiber-optic systems, Gnostic Concepts predicts that fiber-optic connectors will be the fastest growing sector of the connector market. In 1984, 17.5% of the fiber-optic connectors produced were dedicated to in-house use, particularly by providers of voice/data equipment and services. By 1990, the percentage of "captive" production should fall to 10.5%, as standards develop and volume production drives prices down.

AVERAGE ANNUAL GROWTH IN US CONNECTOR AND IC-SOCKET MARKET

CONNECTOR TYPE	PERCENT GROWTH 1984 TO 1990
PRINTED WIRING	12.4
PLANAR CABLE	12.2
RECTANGULAR	6.9
CYLINDRICAL	11.4
COAXIAL	10.9
FIBER OPTIC	32.5
IC SOCKET	13.0
SPECIALTY	10.5

(SOURCE: GNOSTIC CONCEPTS INC)

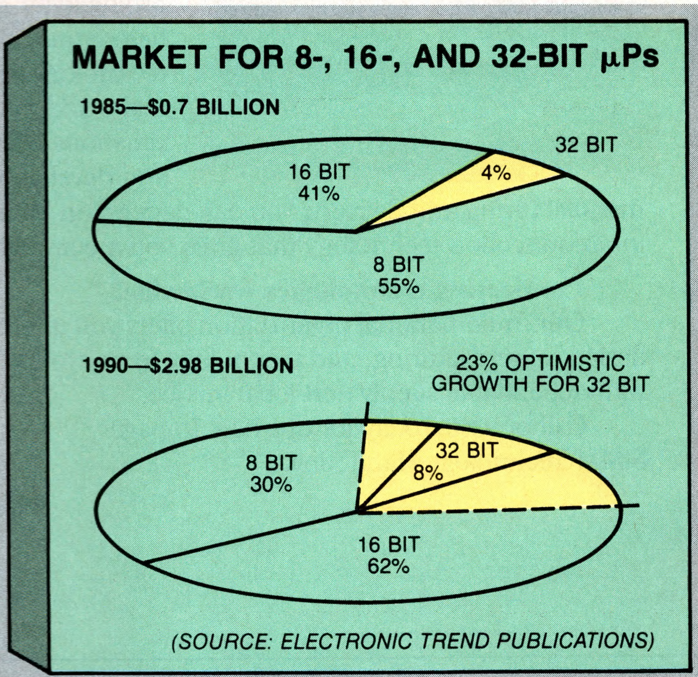
Market for 32-bit µPs may reach $1B by 1990

The extent of their eventual impact remains uncertain in detail, but there is no question that 32-bit µPs will attract the attention of many component manufacturers and systems suppliers over the next few years. Electronic Trend Publications (ETP), a Cupertino, CA, publisher of reports on the electronic industry, believes the market for 32-bit µPs will certainly reach $334 million and may be as high as $1 billion by 1990. This range represents 13 to 39% of the total $2.57 billion µP market.

One measure of the devices' impact is the reclassification of traditional computer categories. The 32-bit µP is the great equalizer, effectively eliminating the distinctions (which were beginning to blur anyway) between mainframes, minicomputers, and microcomputers, and bringing manufacturers of all types of computers into direct competition. The capabilities of even a modest desktop microcomputer based on a 32-bit µP should challenge the energy and imagination of the typical user.

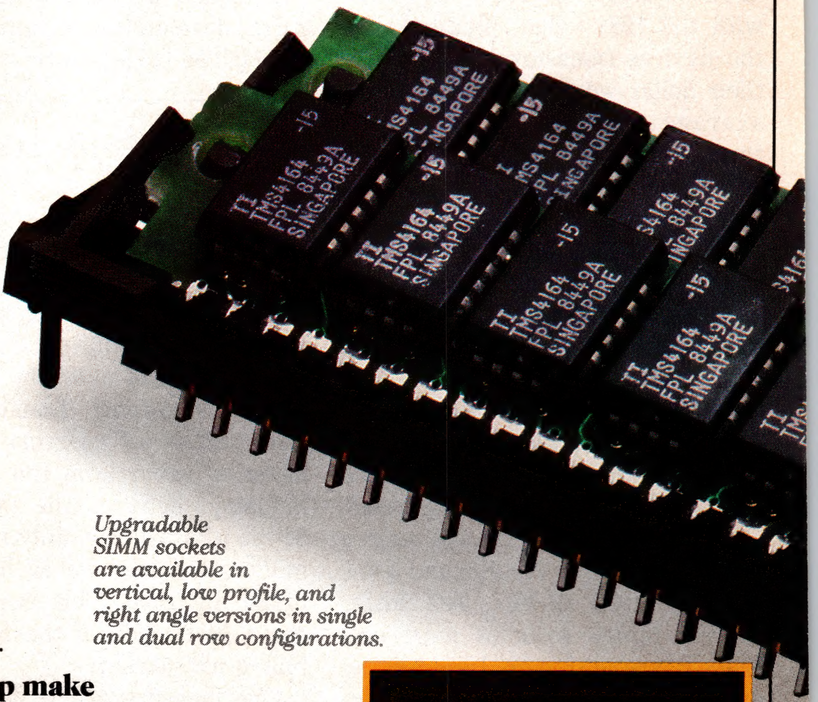
According to ETP, the success of component manufacturers in the 32-bit market will depend on their ability to produce the more complex devices on schedule, on their ability to supplement the devices with support and peripheral chips, on the successful implementation of Unix System V and later versions, and on their ability to garner third-party support for essential system software.

ETP believes that, for systems suppliers, the question is not whether to develop a 32-bit µP-based product line, but rather which processor to choose. Choosing the right processor family is essentially a wager on a variety of factors such as compatibility with 16-bit µPs, coprocessor support, ease of design, and market trends.



Making the Connection Between...

PACKAGING & PRODUCTIVITY



Upgradable SIMM sockets are available in vertical, low profile, and right angle versions in single and dual row configurations.

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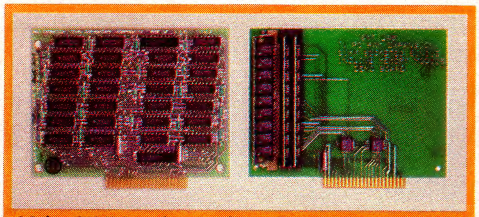
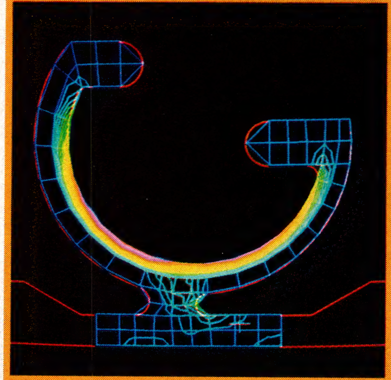


Molex SIMM socket (right) takes up dramatically less board space than DIP packaging (left).



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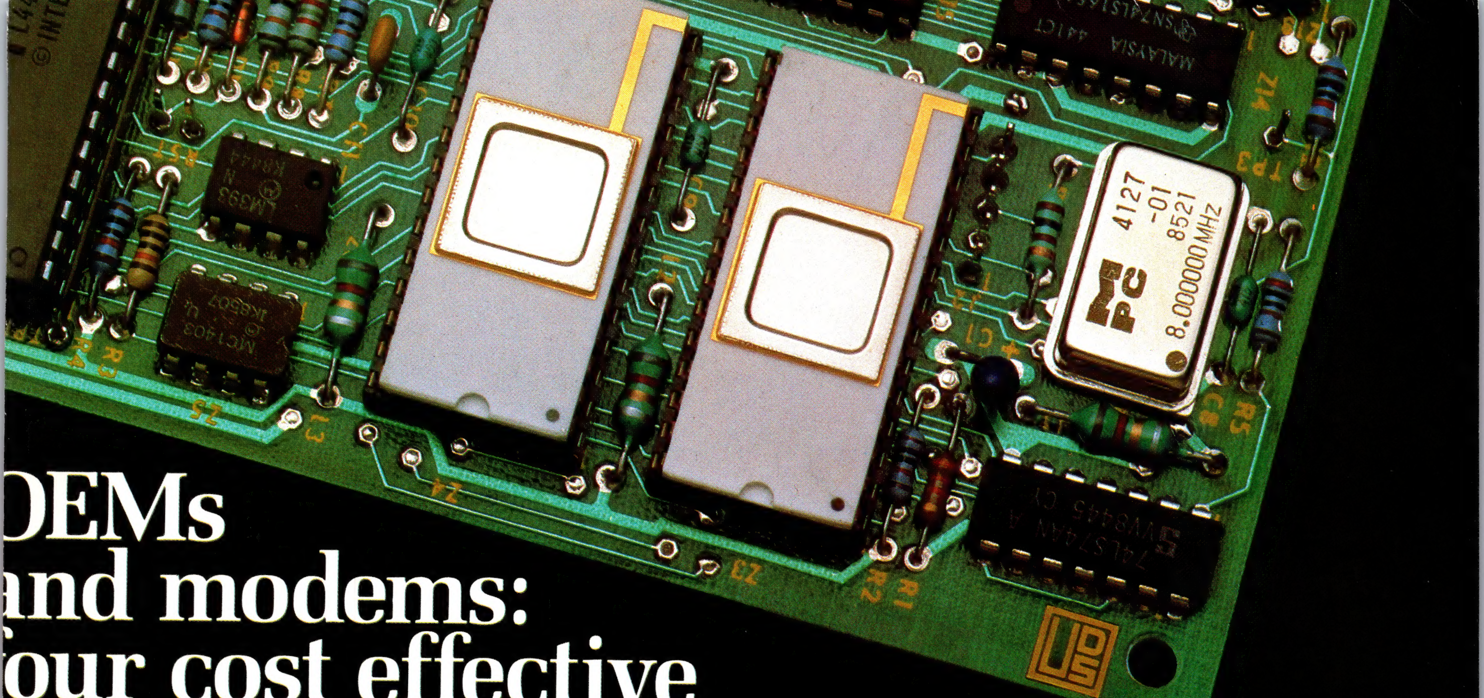

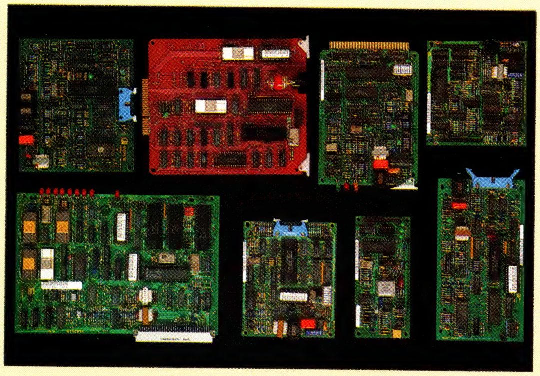

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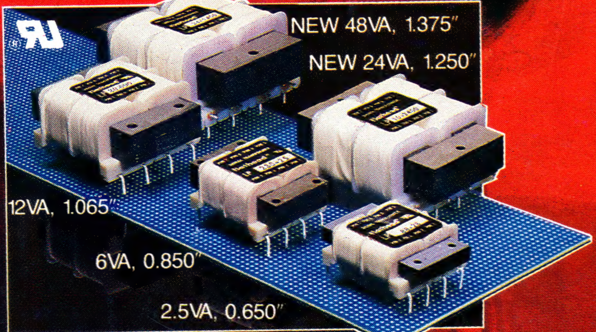

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